

ZQ5 SYSTEM BLOCK DIAGRAM

BOM MARK
IV@: INT VGA
EV@: STUFF FOR EXT VGA
SP@: STUFF FOR UMA or VGA

REV:A

DDR3 PWR TPS51116 P36	CHARGER ISL6251 P32
THERMAL PROTECTION P40	3/5V SYS PWR ISL6237 P33
DISCHARGER P39	CPU CORE PWR OZ8116LN P35
VGA CORE OZ8118 P37	+1.05V UP6111AQDD P34

CLOCK GENERATOR
ICS:
SELGO: SLG8SP513VTR P2

XTAL
14.318MHz

Penryn 478
uFCPGA P3, P4

Thermal Sensor
(G780P81U) P3

Fan Driver
(G991) P25

DDRIII
SO-DIMM 0
SO-DIMM 1 P16,P17

NB Cantiga
(GM45/ PM45/ GL40)
P5, P6, P7, P8, P9, P10, P11

ATI-Park
VRAM DDRIII
512MB P18-P23

SWITCH CIRCUIT P25

HDMI switch (PS8101T) P25

CRT P24

LVDS P24

HDMI P25

HDD (SATA) *1 P26

ODD (SATA) P26

Ext USB Port x 2
USB 0,2 P27

Int USB Port x 1
USB 6 P27

Bluetooth
USB3 P27

CCD
USB11 P24

SB ICH9M
P12,P13,P14,P15

PCI-Express

PCI-E-4

Mini Card WLAN P27

Audio CODEC (272) P28

EC (WPC781) P33

Media Cardreader (AU6437)
USB2 P30

Giga-LAN BCM57780 P30

Audio Amplifier G1453L P28

MIC Jack P29

Int. MIC P29

Int. Speaker P29

SPI ROM P33

Touch Pad P26

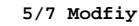
K/B COON. P33

Card Reader Connector P32

Transformer P31

RJ45 P31

02



Default

SLG8SP513VTR ,ICS9LPRS365BKLFT

3V PCLK_DEBUG_R

R329 10K 4

R331 *10K 4

3V PCLK_591_R

R336 EV@10K 4

R332 IV@10K 4

HIGH 27MHz
LOW SRC

3V PCLK_ICH_R

R342 *10K 4

R343 10K 4

To NB

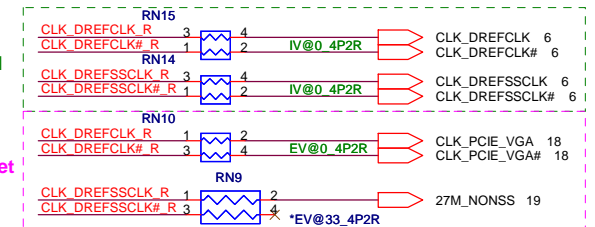
3 CPU_BSEL0 R347 0 4 MCH_BSEL0 6

3 CPU_BSEL1 R267 0 4 MCH_BSEL1 6

3 CPU_BSEL2 R315 0 4 MCH_BSEL2 6

5/18 Modifv

<MAIN>:ICS9LRS3165BKLF QCI:ALPRS365000
<SECOND>:SLG8SP513VTR QCI:AL8SP513000
<SECOND>:RTM875N-606-VD-GRT QCI:AL000875000

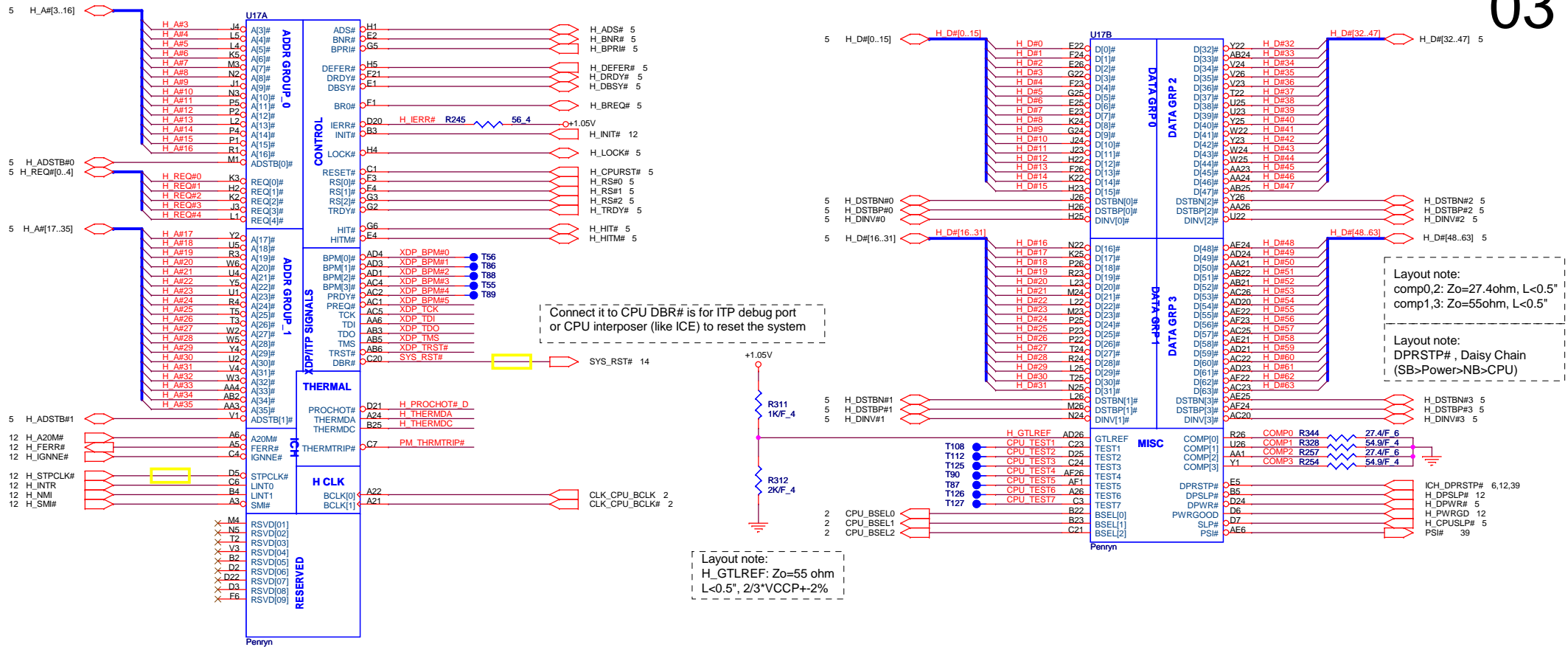


5/22 modify

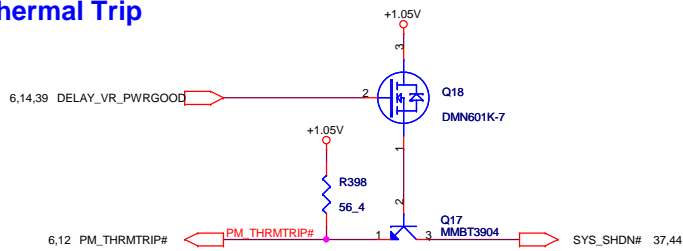


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Quanta Computer Inc.

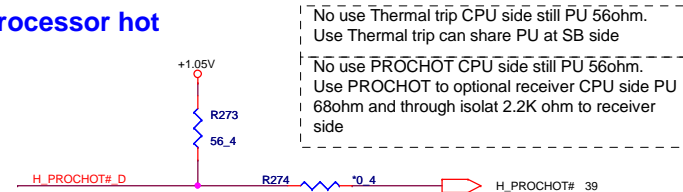
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Thermal Trip

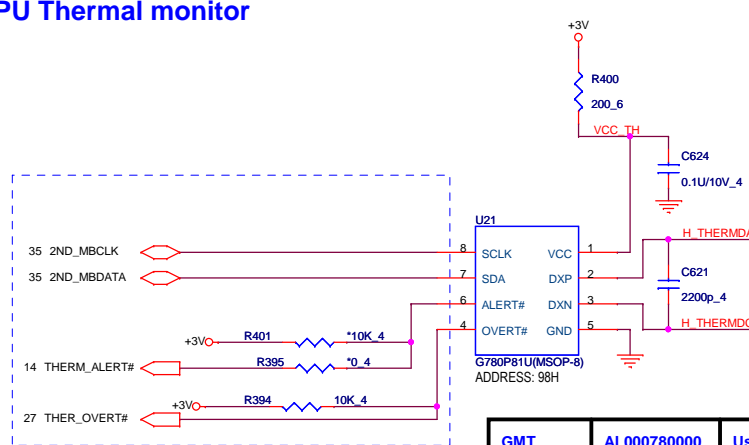


Processor hot

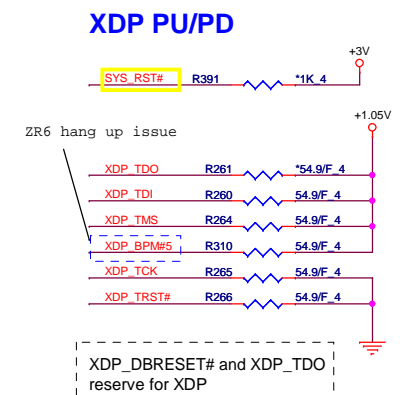


CPU 1/2

CPU Thermal monitor



XDP PU/PD

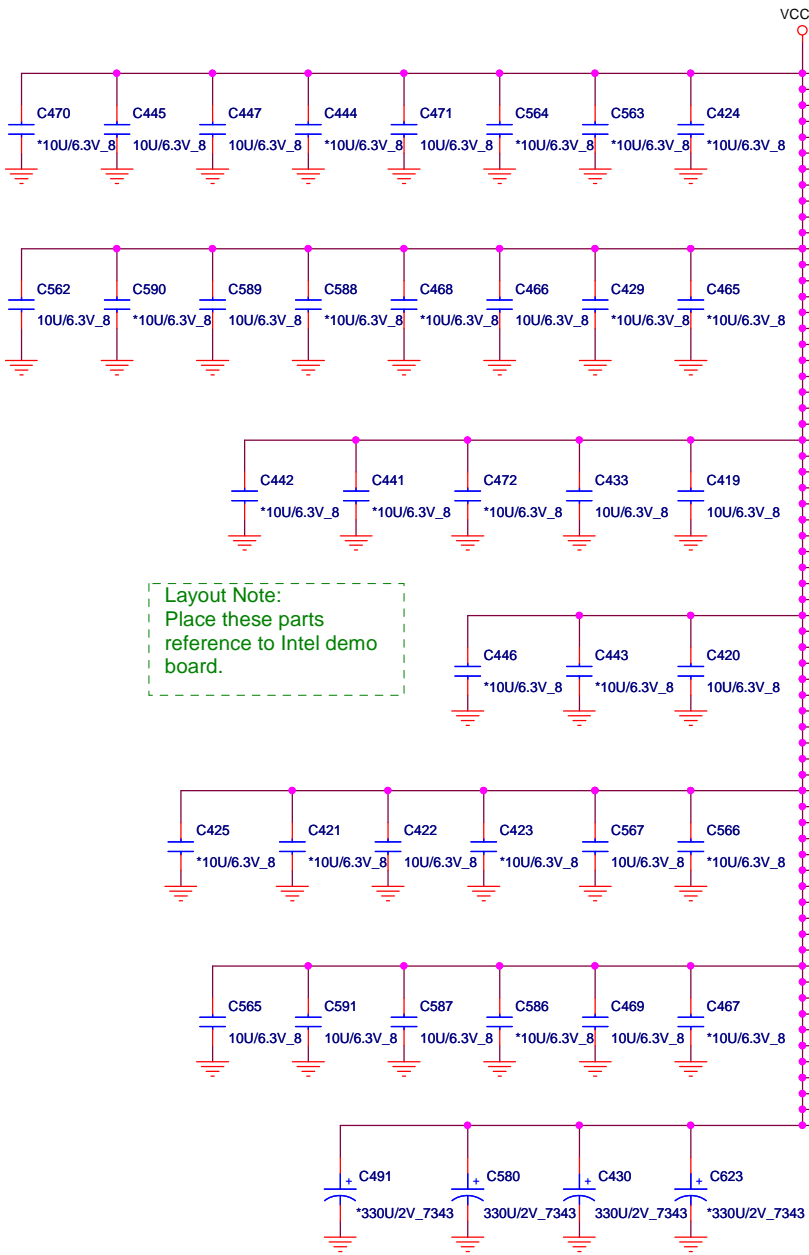
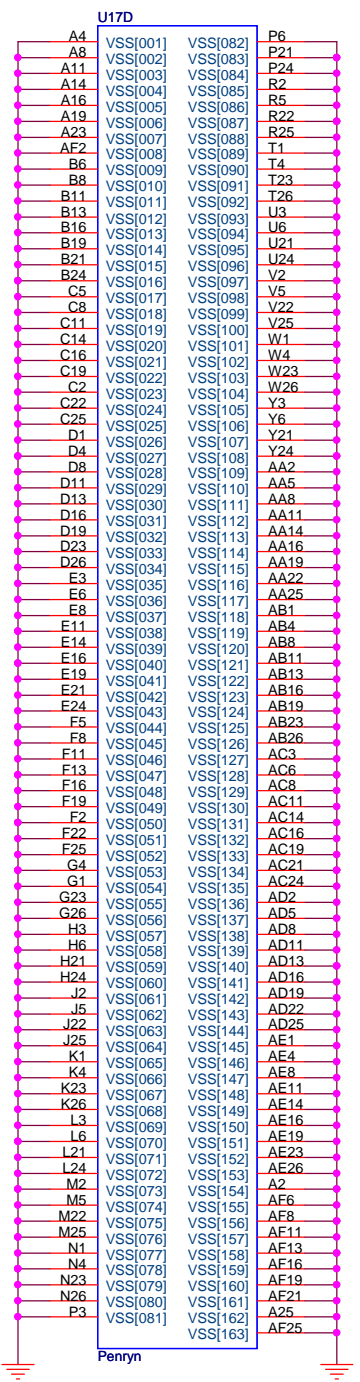


GMT	AL000780000	Use 2200p
NS	AL095245000	Use 2200p
WINDBOND	AL83L771K01	Use 2200p



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Size	Document Number	Rev
	CPU Host Bus	1A
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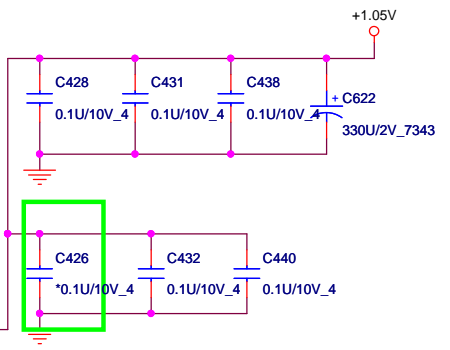


Layout Note:
Place these parts
reference to Intel demo
board.

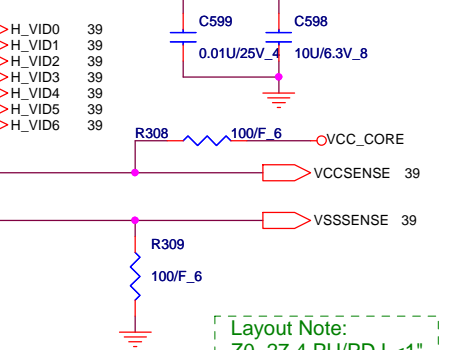
VCC:38A (Low power type)
VCC:47A (Standard type)

Layout Note:
Inside CPU center cavity in 2 rows

VCCP : 2.5A(Supply after VCC Stable)
4.5A(Supply before VCC Stable)



VCCA:130mA



Layout Note:
Z0=27.4,PU/PD L<1"

Montevina platform : Early Reference Board Schematics Feb 2007. Rev 1.0
stuff 22U*34, NC 22U*2
stuff 330U*2, NC330U*2

CPU 2/2

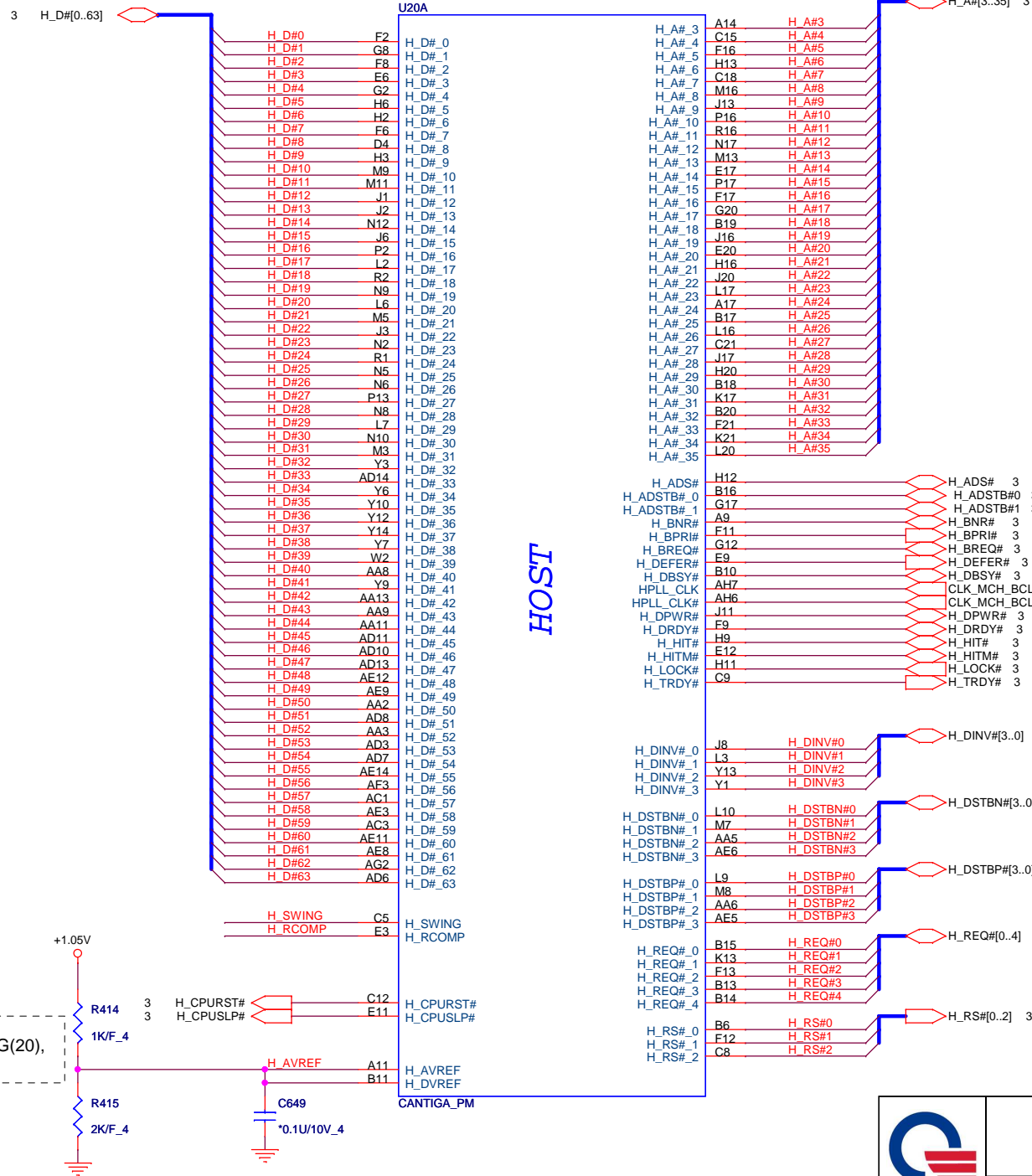
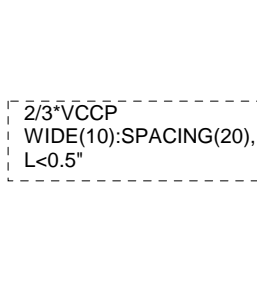
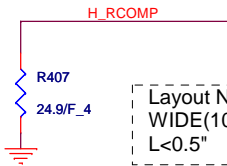
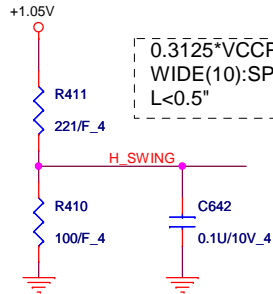
PROJECT : ZQ5
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Size	Document Number	Rev
	CPU Power	1A
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GMCH (CANTIGA)

05

	QCI P/N
Intel Cantiga (G)M	AJSLB940T04
Intel Cantiga (P)M	AJSLB970T06
Intel Cantiga (G)L A1	AJSLGGM0T04



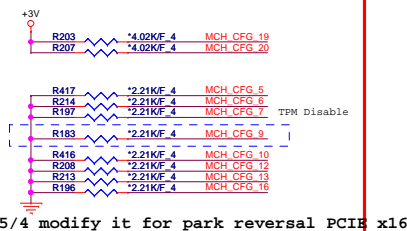
PROJECT : ZQ5
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Size	Document Number	Rev
	GMCH HOST	1A
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Strap table

Pin Name	Strap description	Configuration
CFG2[2:0]	FSB Frequency Select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG4[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIe Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIe Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG15[14:1]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG18[17:1]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI) and Concurrent with PCIe	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIe is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI Device Present(Default) 1 = SDVO/HDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent (Default) 1 = Digital display(HDMI/DP) device present

Strap pin



5/4 modify it for park reversal PCIe x16

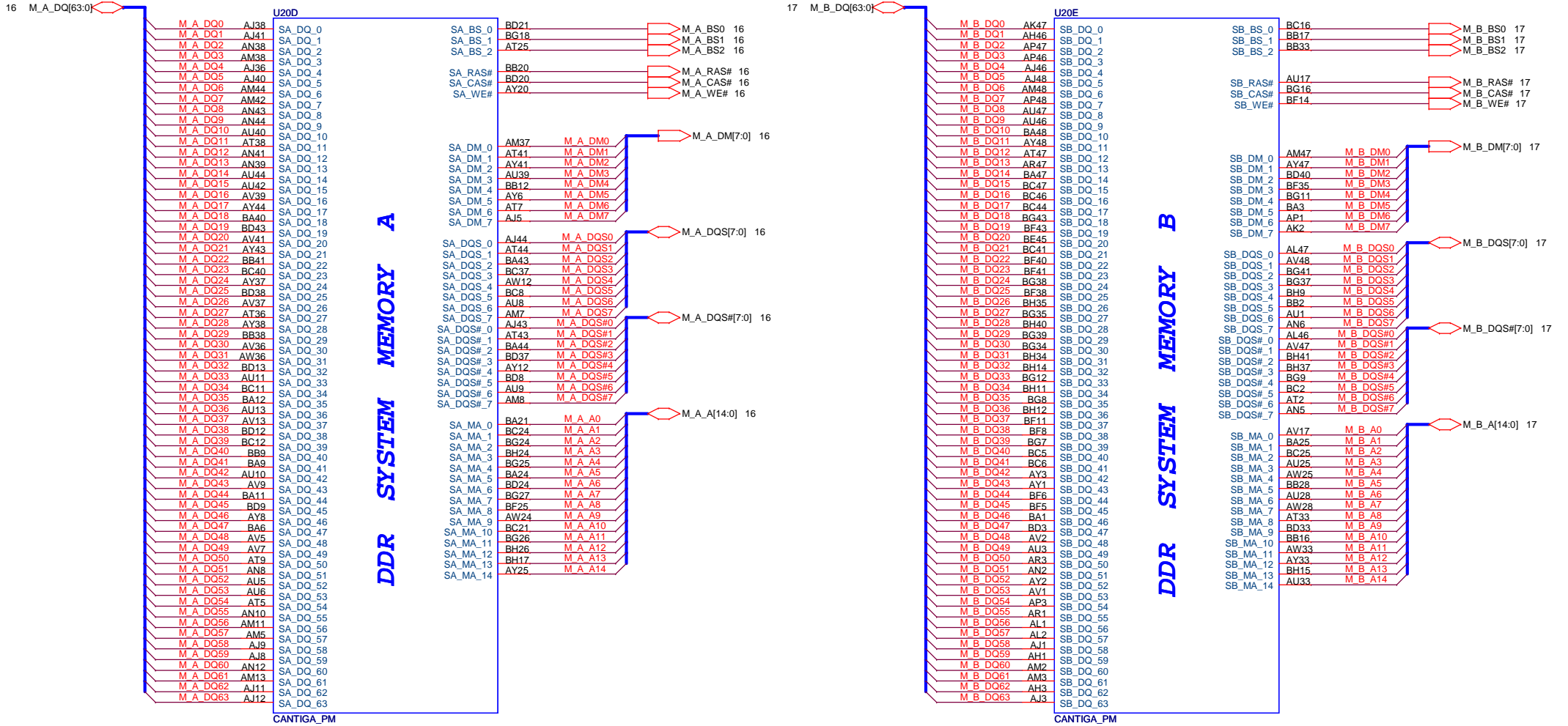


NB Thermal trip pin
No use Thermal trip NB side can
NC (NB has ODT)

PM DPRSTP#
The Daisy chain topology should
be routed from ICH9M to IMVP,
then to (GMCH and CPU, in that
order.

U20B
RSDV01
RSDV02
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Date:	Friday, May 28, 2010	Sheet 7 of 43
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Power consumption reference to Intel
644135 Cantiga chipset EDS Volume1.
Section 10

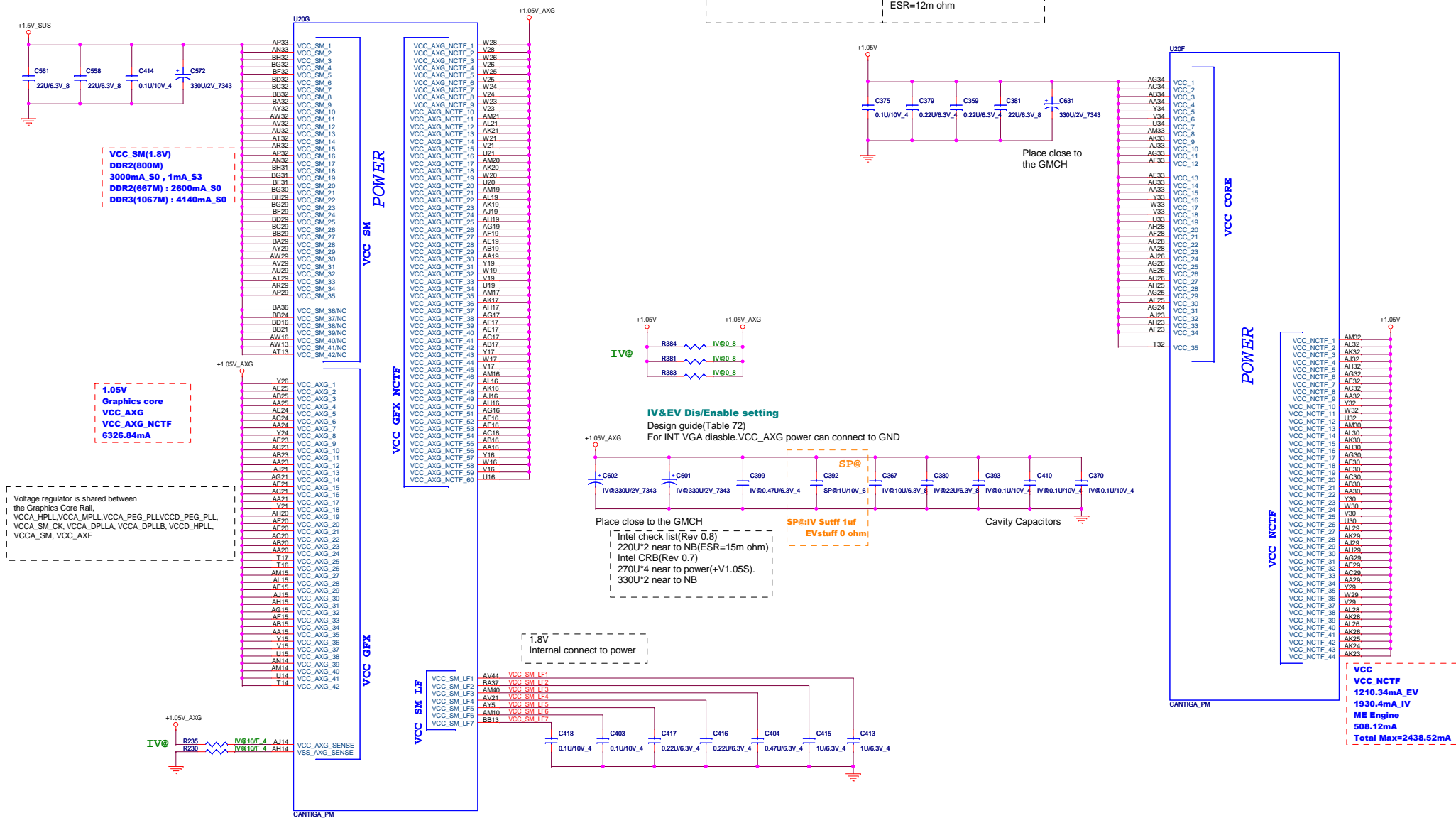
GM	TDP	10.5~12W
GS	TDP	7~8W
PM	TDP	7W

Intel check list(Rev 0.8)
No description for VCC_SM bulk CAP
Intel CRB(Rev 0.7)
330U*1 Reserve near to power
330U*1 near to NB

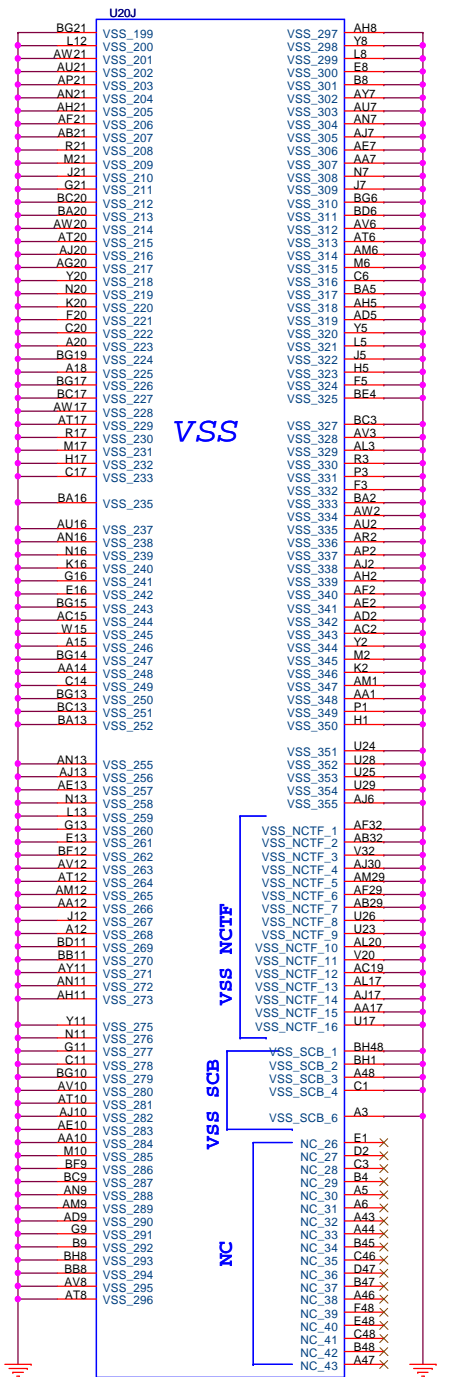
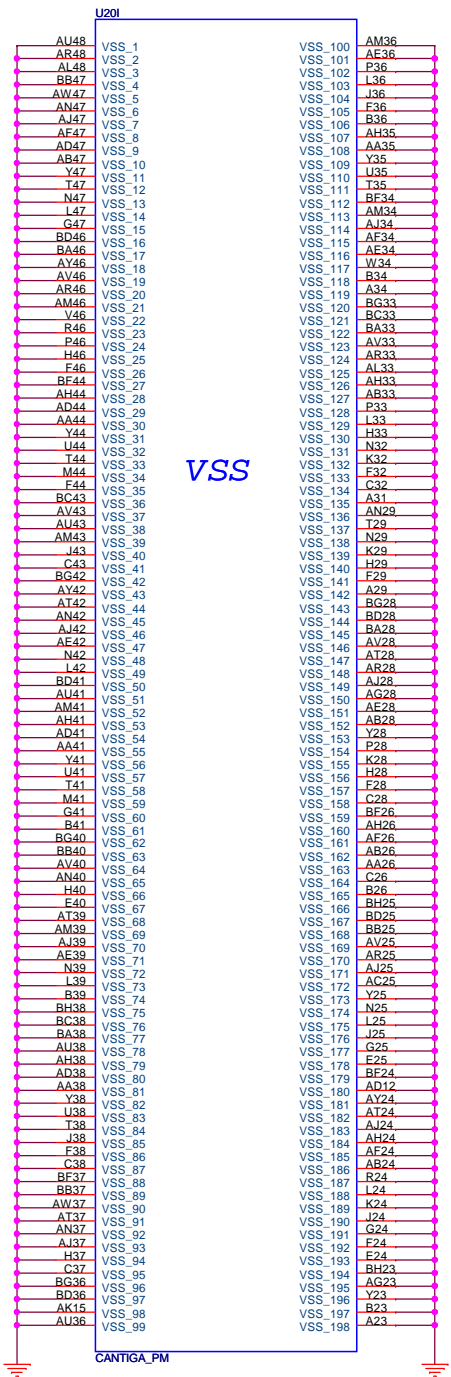
```

Intel check list(Rev 0.8)
270U*1 near to power(+V1.05M).
270U*2 near to NB
Intel CRB(Rev 0.7)
270U*3 near to power(+V1.05M).
270U*1 near to NB
ESR=12m ohm

```



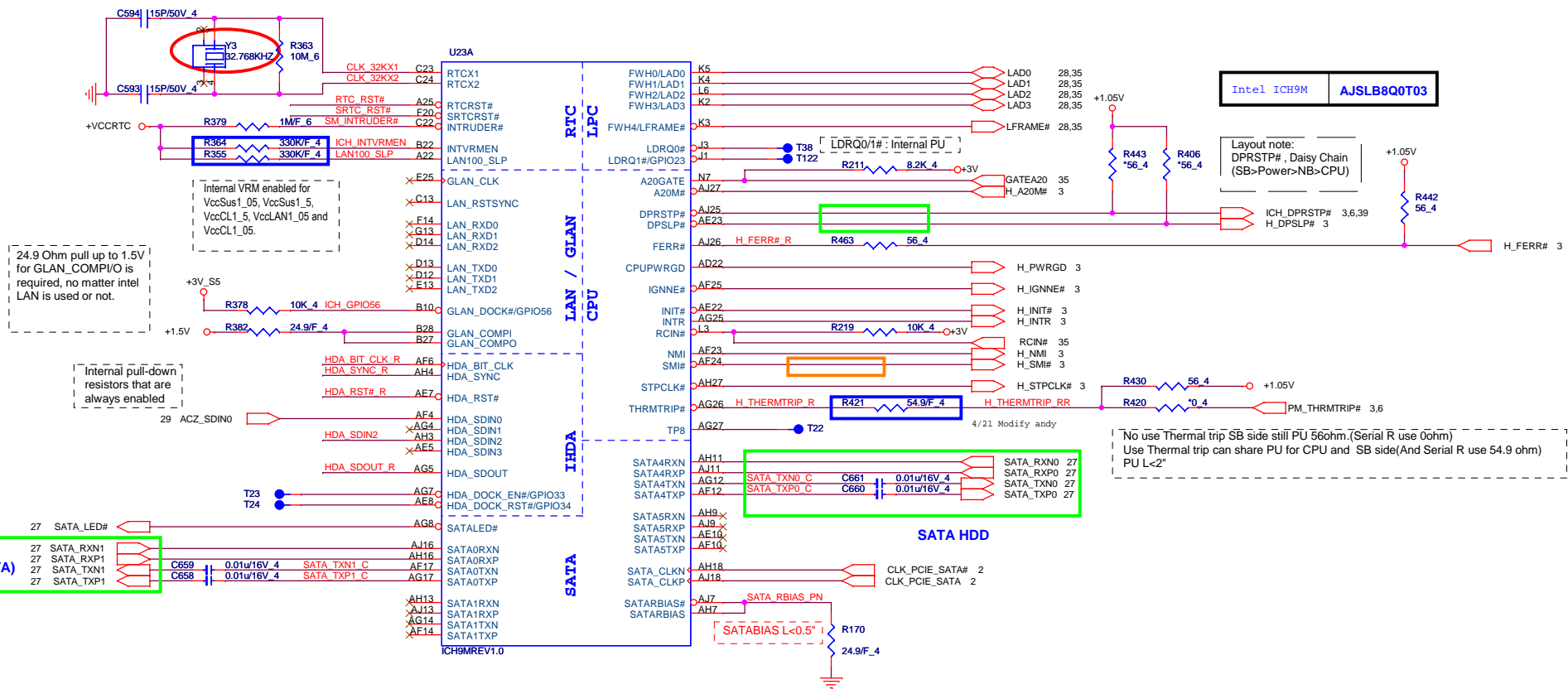
1. Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially
2. VCC_AXG_SENSE PU to +V GFX_CORE_INT with 10ohm and VSS_AXG_SENSE PD with 10ohm for Intel suggest



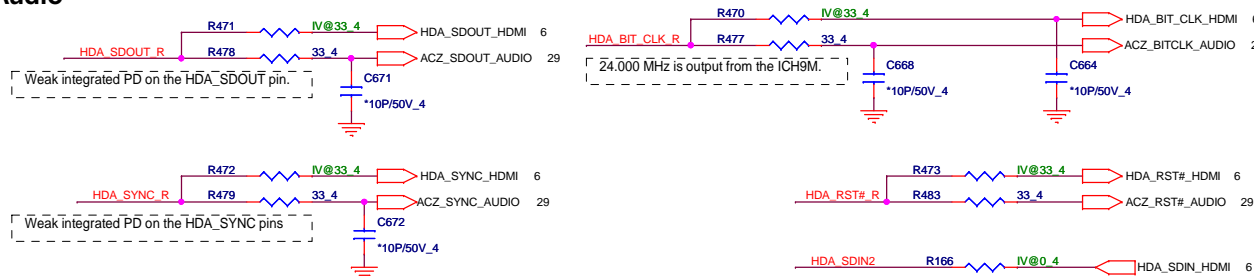
ICH9M

IV@

EV@



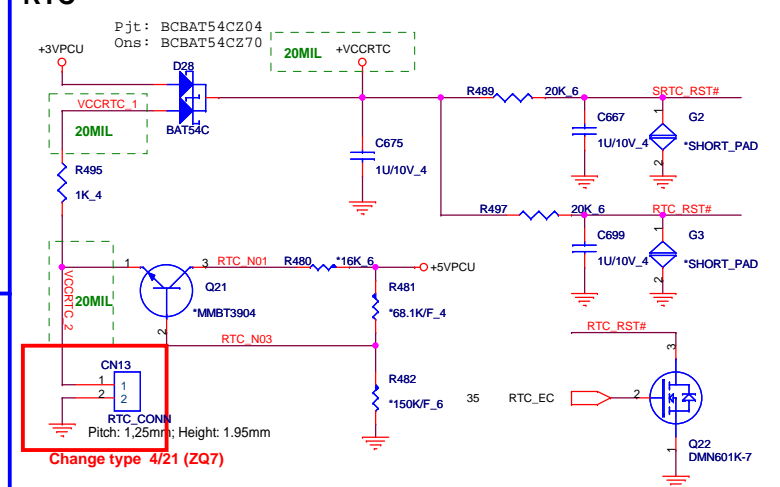
HD Audio



South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration			PU/PD	
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect			This strap should only be enabled in manufacturing environments using an external pull-up resistor.	
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU				
TP3	XOR Chain Entrance	PWROK	ICH_TP3	HDA_SDOUT	Description	14	
			0	0	RSVD		
			0	1	Enter XOR Chain		
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK	1	0	Normal operation(Default)		
			1	1	Set PCIe port config bit 1		





RTC

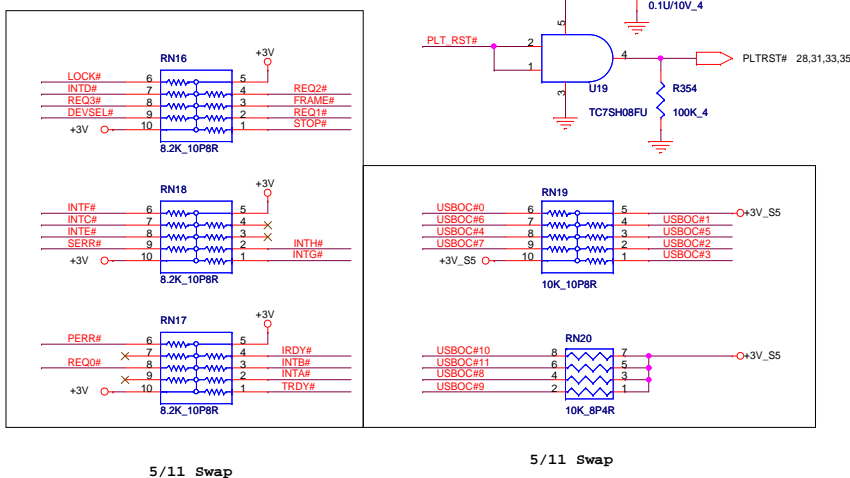


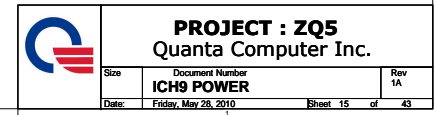
PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	ICH9M HOST	1A
Date:	Friday, May 28, 2010	Sheet 12 of 43



Pin Name	Strap description	Sampled	Configuration			PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0			
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default			
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default			
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default			
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable			
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0	SPI_CS#1	Boot Location	
			0	1	SPI	
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	1	0	PCI	
			1	1	LPC(Default)	

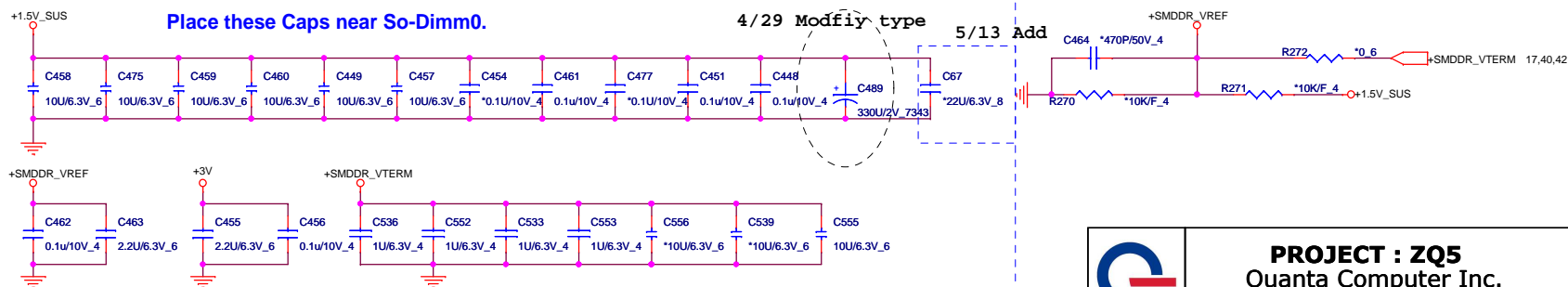
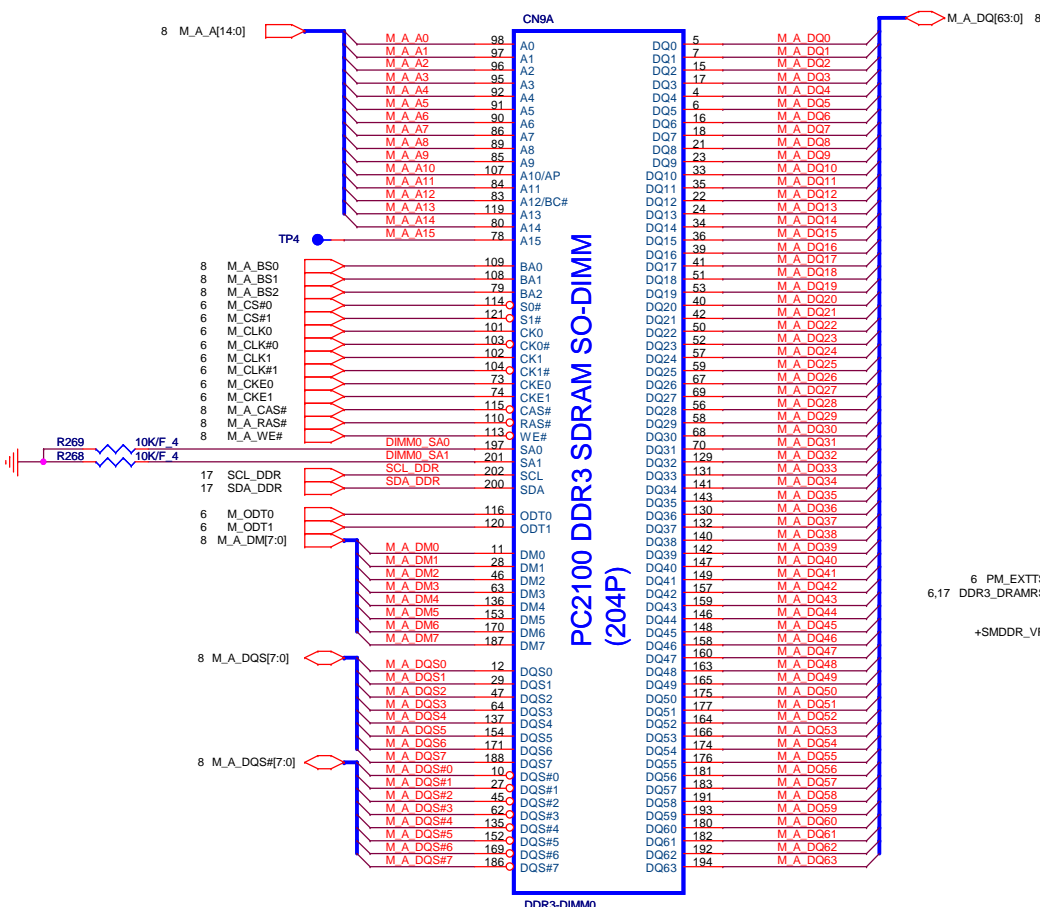
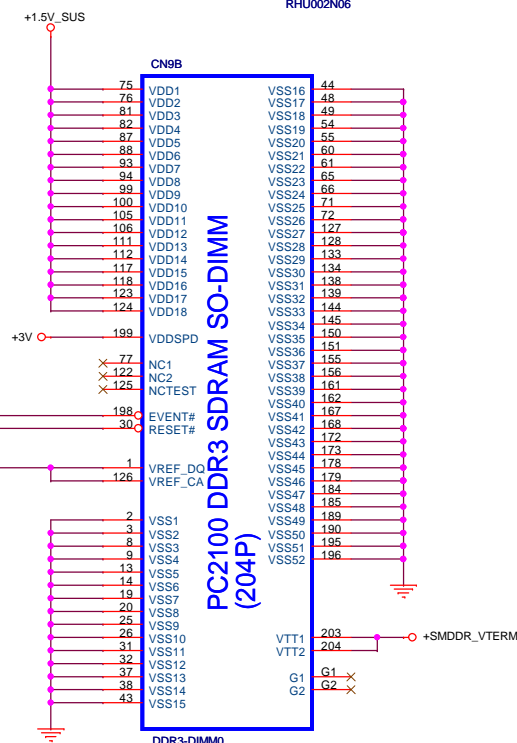
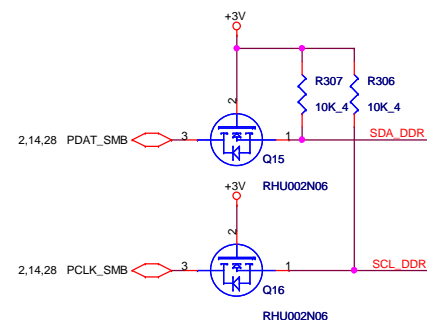




DDR3 (DDR)

STD H=4.0 MM	QCI P/N
LTK	DGMK4000004
FOX	DGMK4000117

16



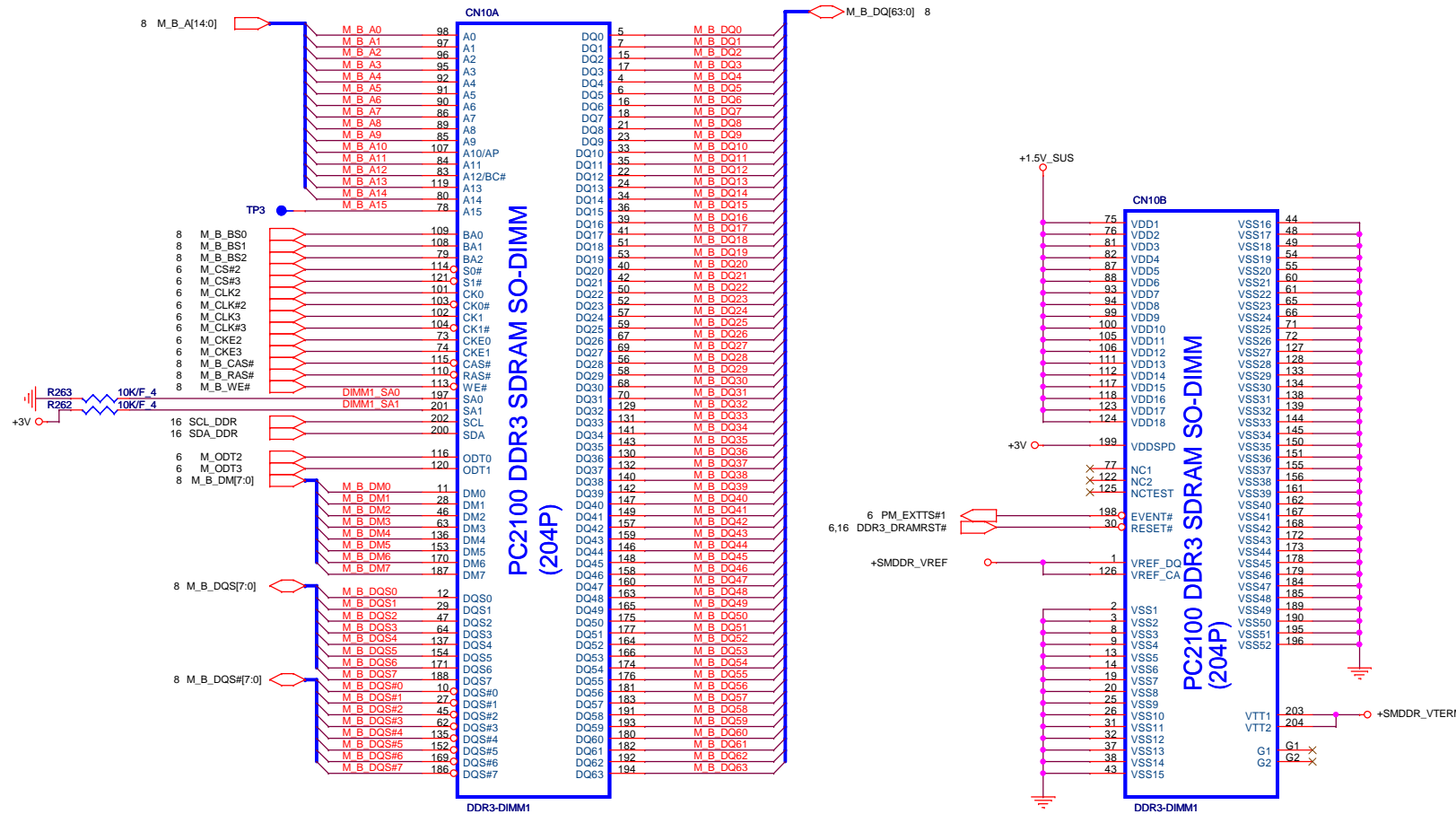
PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number DDR3 DIMM-0(H=5.2)	Rev 1A
Date:	Friday, May 28, 2010	Sheet 16 of 43

DDR3 (DDR)

STD H=8.0 MM	QCI P/N
LTK	DGMK4000097
FOX	DGMK4000130

17



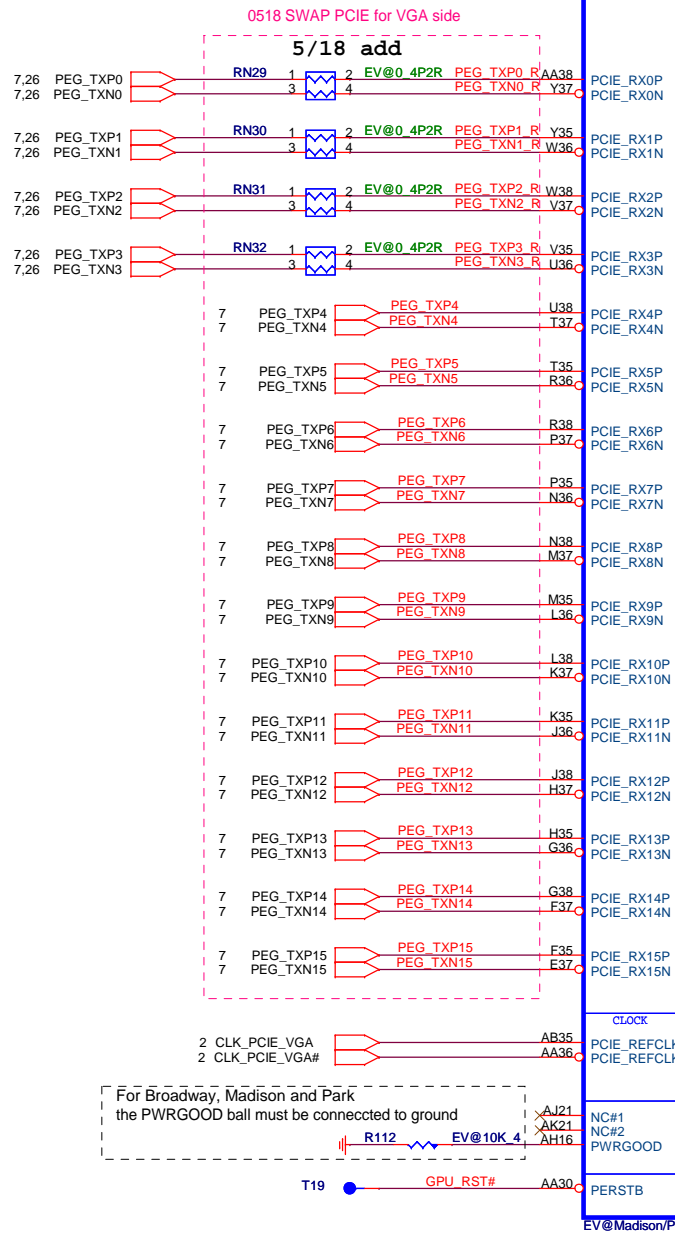
Place these Caps near So-Dimm1.

5/6 Modfiy

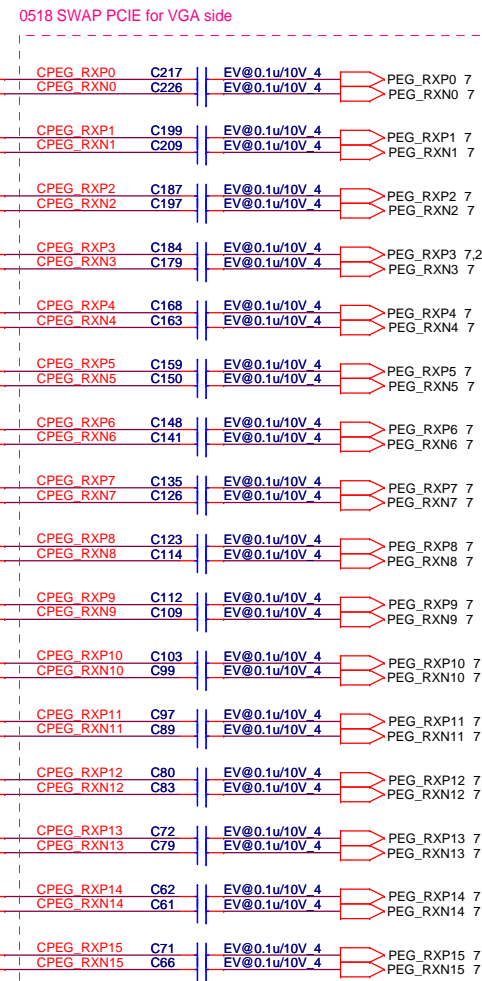


PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	DDR3 DIMM-1(H=9.2)	1A
Date:	Friday, May 28, 2010	Sheet 17 of 43



PCI EXPRESS INTERFACE



Item	Quanta P/N
Park	AJ077400T08
Robson	AJ007740T02

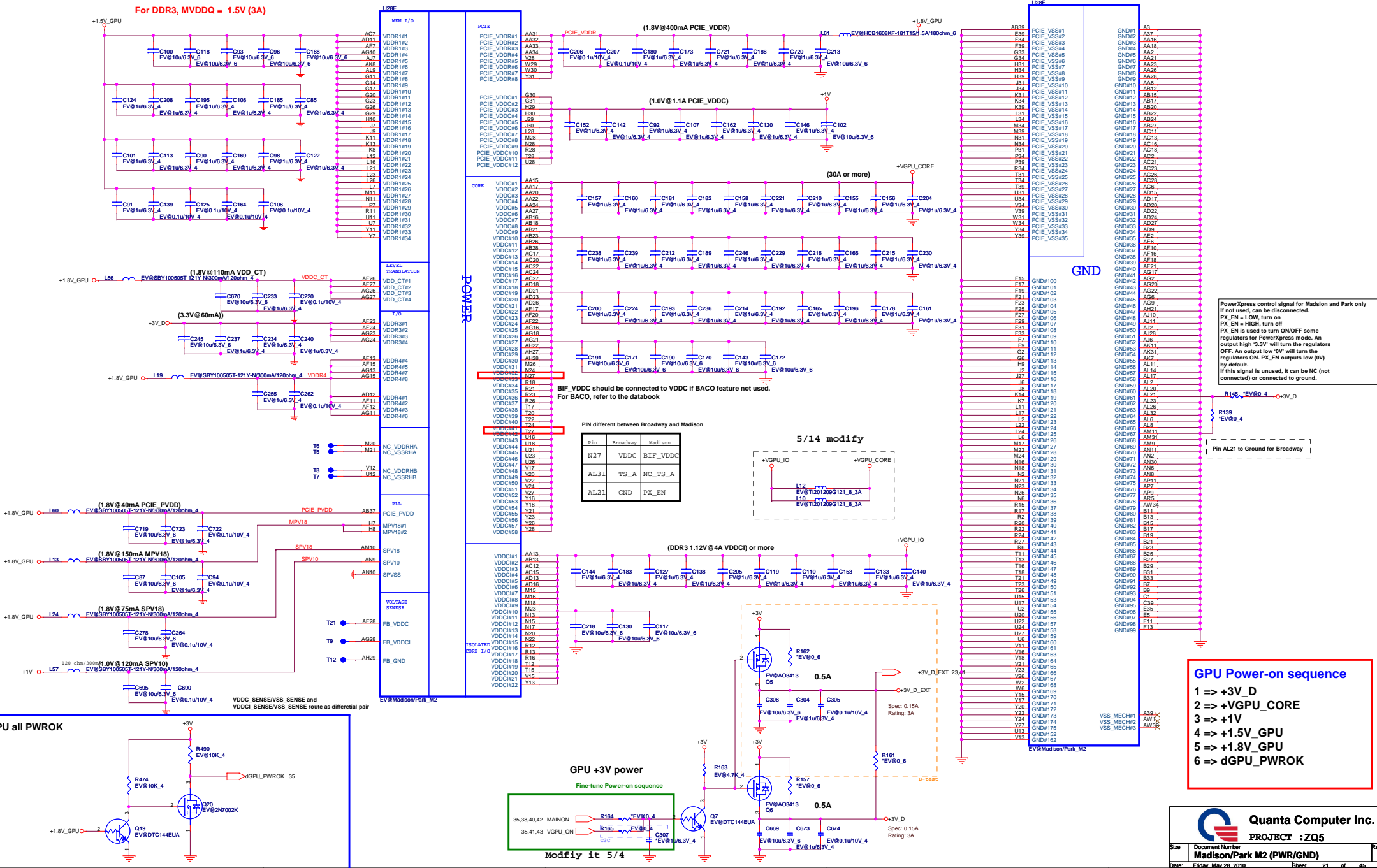


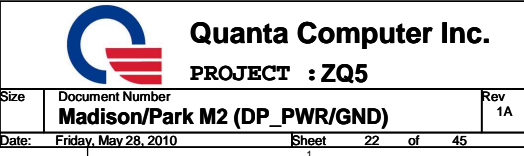
Quanta Computer Inc.
PROJECT : ZQ5

Size	Document Number	Rev
	Madison/Park M2-PCIE I/F	1A
Date:	Friday, May 28, 2010	Sheet 18 of 45

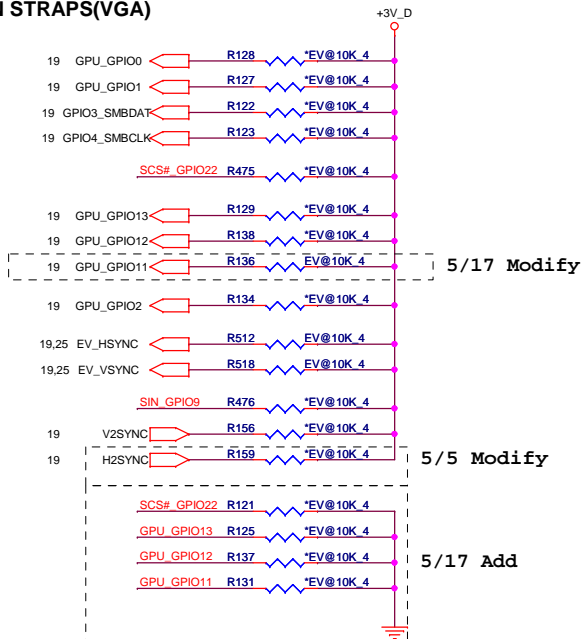
GPU_4(VGA)

For DDR3, MVDDQ = 1.5V (3A)





PIN STRAPS(VGA)



ROM Table	
Size of the primary memory apertures	CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
32 MB	011

ROM Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

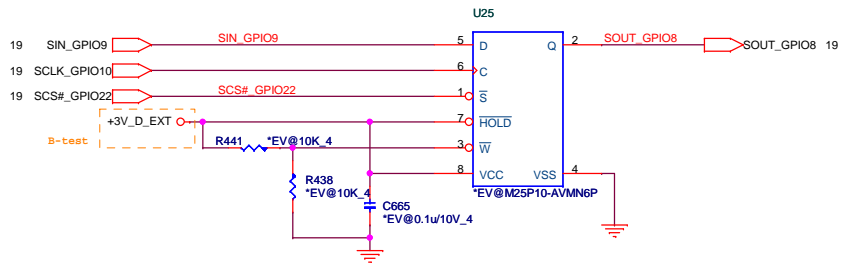
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	1	
ROMIDCFG(2:0)	GPIO[13:11]	Primary Memory Aperture size requested at PCI Configuration	001	table 3-35
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

23

EEPROM(VGA)

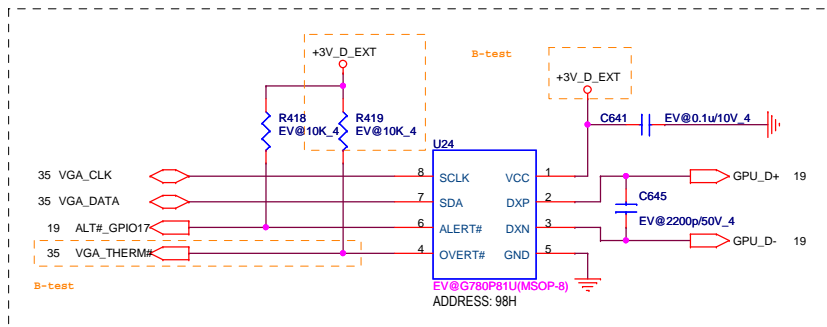


Thermal Sensor(VG

Vendor	P/N
WINDBOND	AL83L771K01
GMT	AL000780000

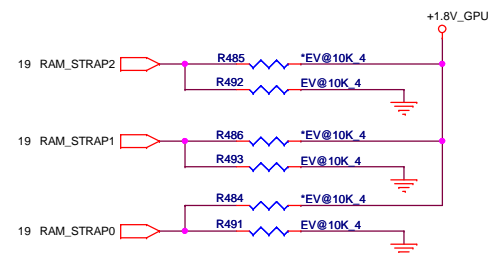
USD0.16

5/6 modify



DDR3 Memory Aperture size(GPU)

DDR3 Memory Aperture size					
Vendor	Vendor P/N	STN B/S P/N	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix			1	1	0
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1	0	0
			1	0	1
Samsung					
	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500 (128M*16)	0	0	1



```
RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.
```

**Quanta Computer Inc.**

PROJECT : ZQ5

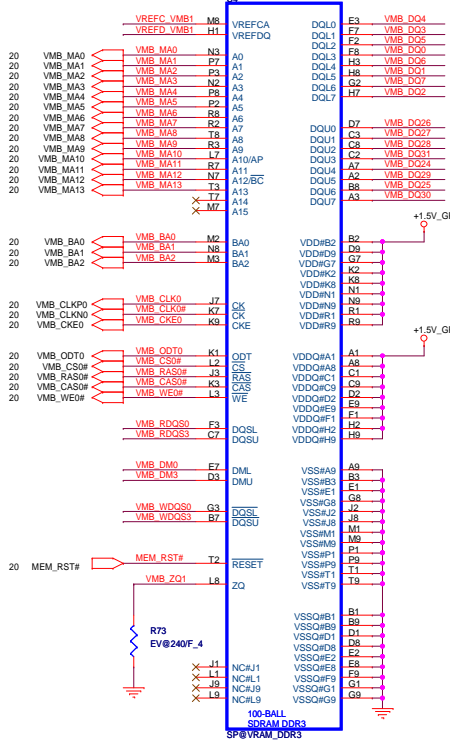
Size	Document Number Strip/Thermal	Rev 1A
Date:	Friday, May 28, 2010	Sheet 23 of 45

CHANNEL B: 512MB DDR3 (16*64M*4pcs)

24

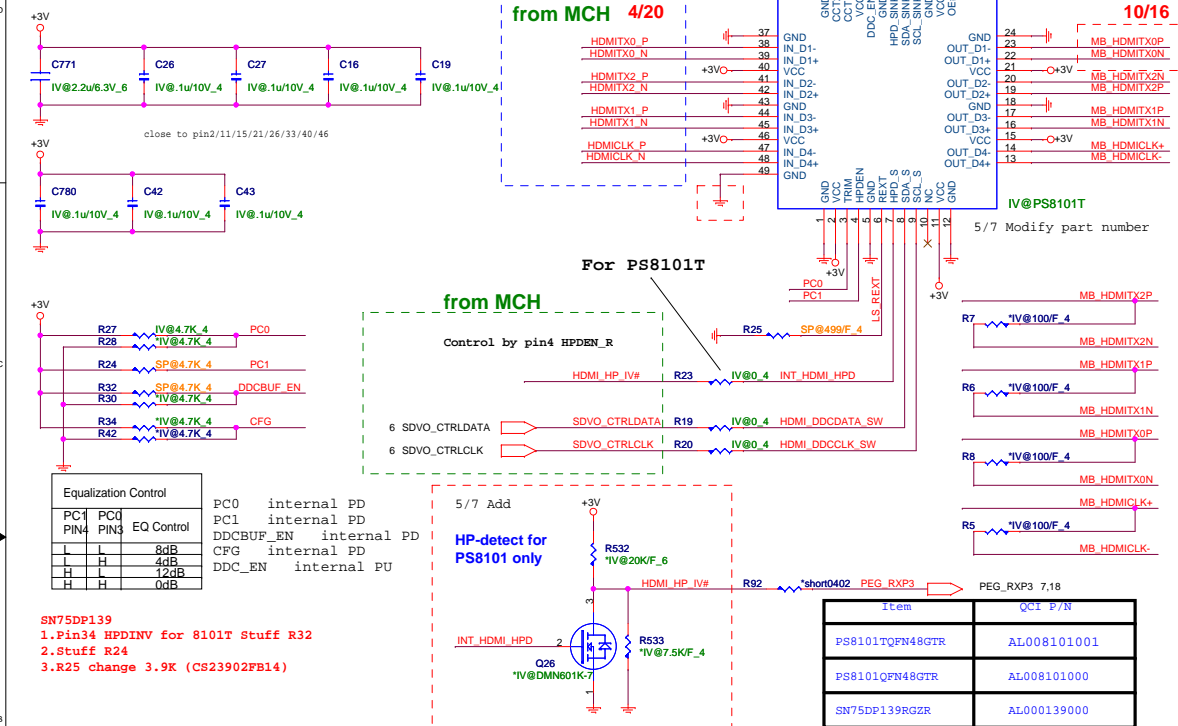
20 VMB_DQ[63..0]
20 VMB_DM[7..0]
20 VMB_RDOQ[7..0]
20 VMB_WDOQ[7..0]

QSA[7..0]
QSA# [7..0]

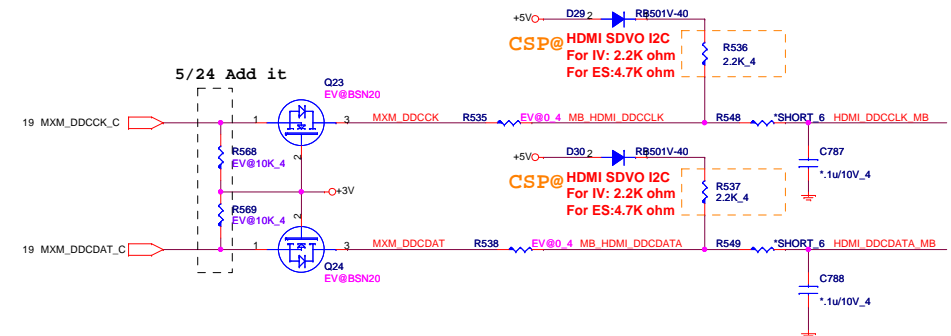


IGPU HDMI LEVEL SHIFTER

IV@ --> iGPU only
EV@ --> dGPU only

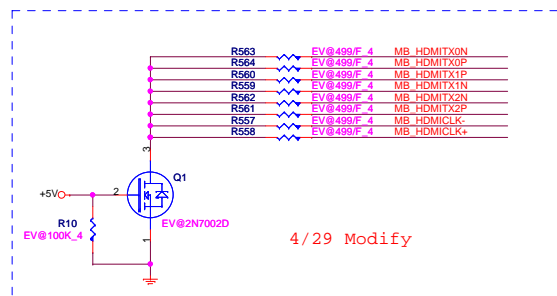


SDVO I2C Control

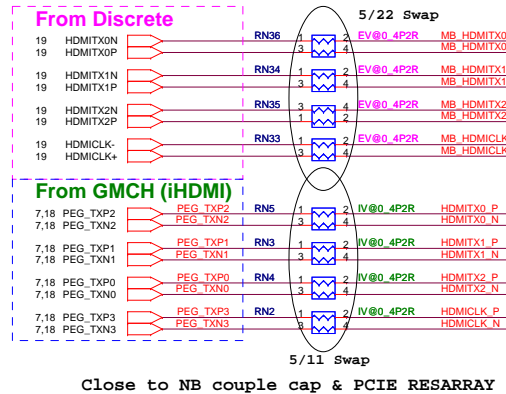


GPU Switchable Graphic HDMI source

To Discrete

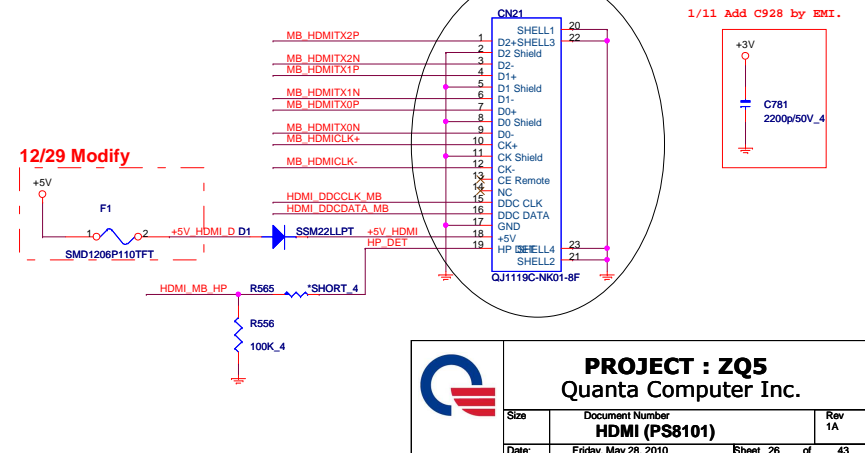


Close to HDMI connector

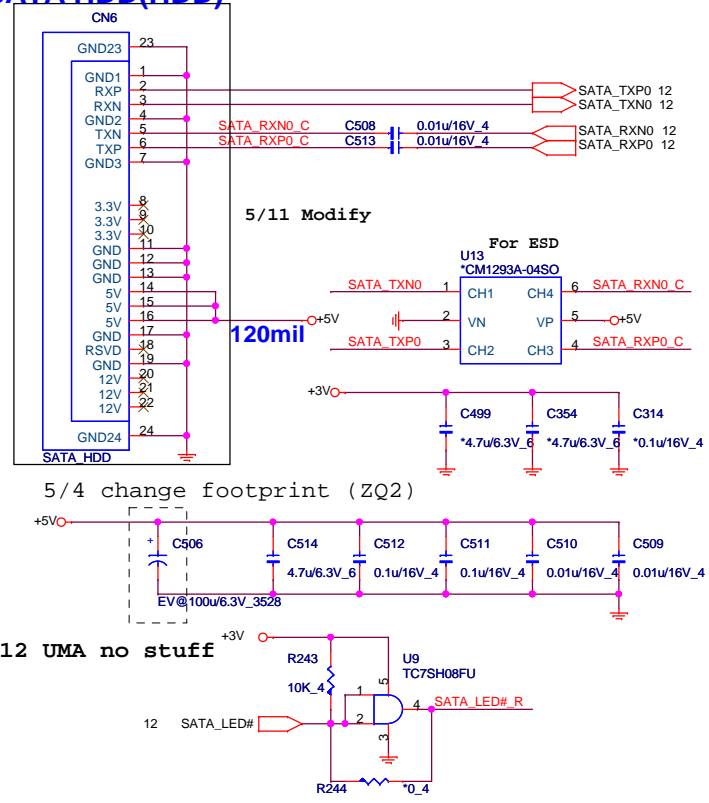


HDMI connector

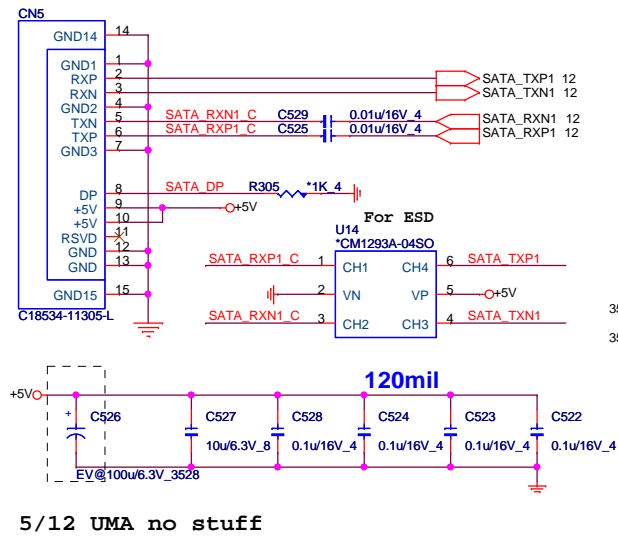
update footprint 4/19 ZQ2



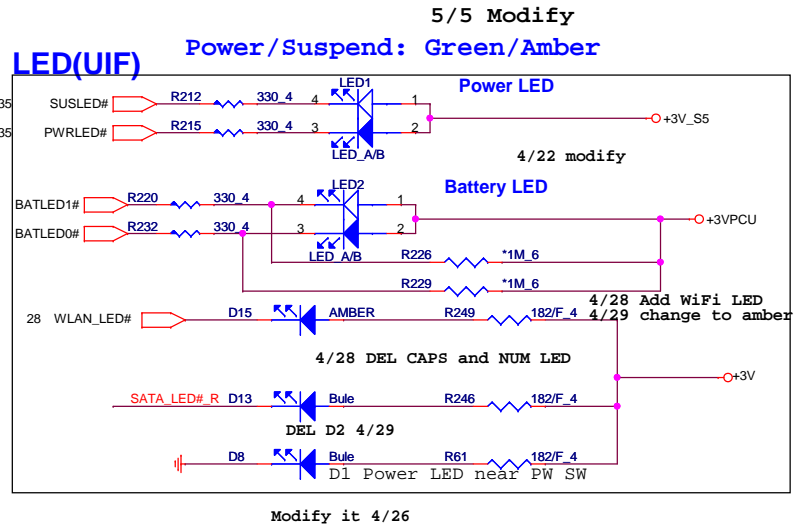
SATA HDD(HDD)



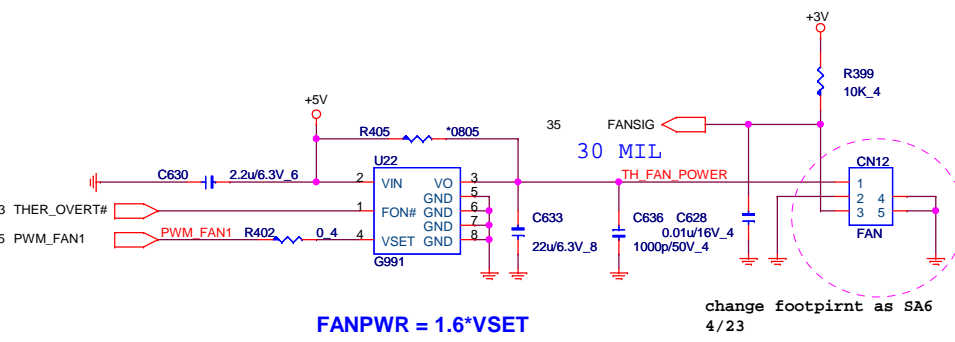
SATA ODD(ODD)



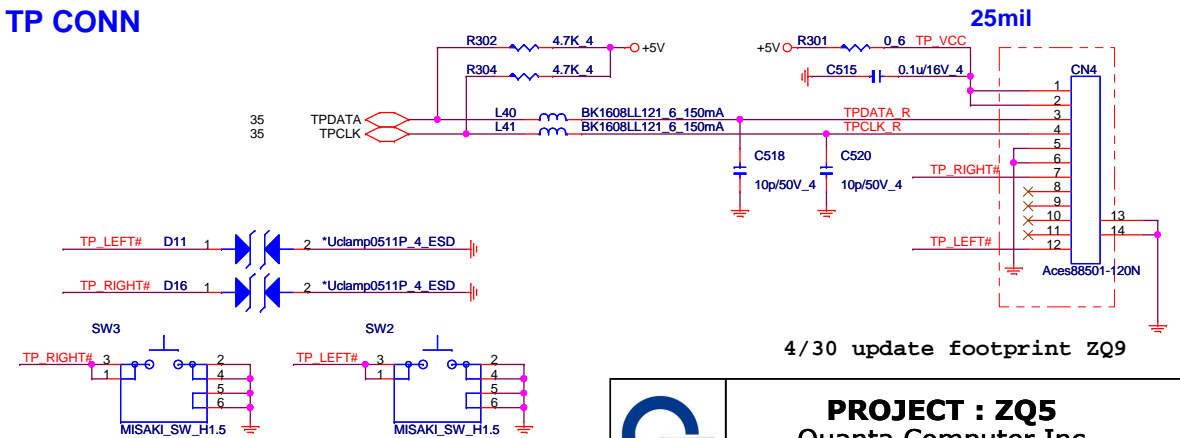
LED(UIF)



FAN(THM)



TP CONN

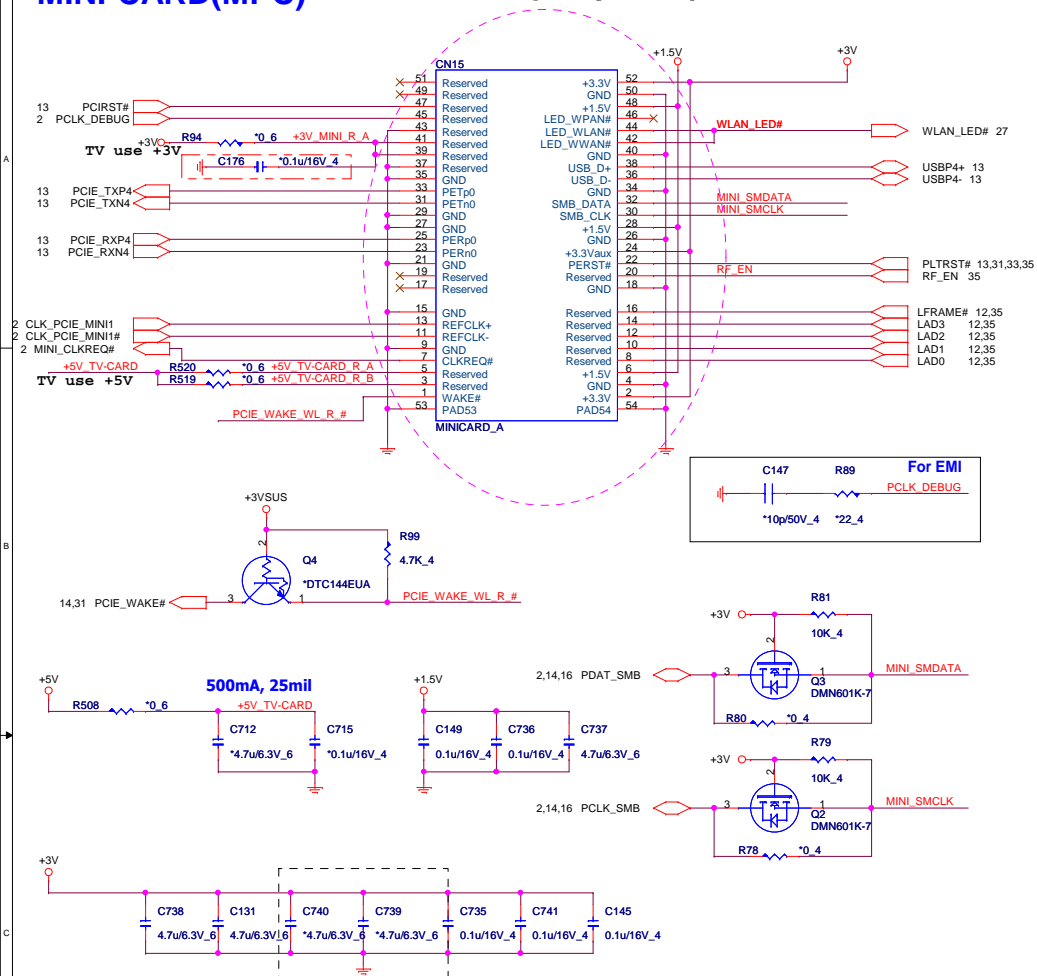


PROJECT : ZQ5
Quanta Computer Inc.

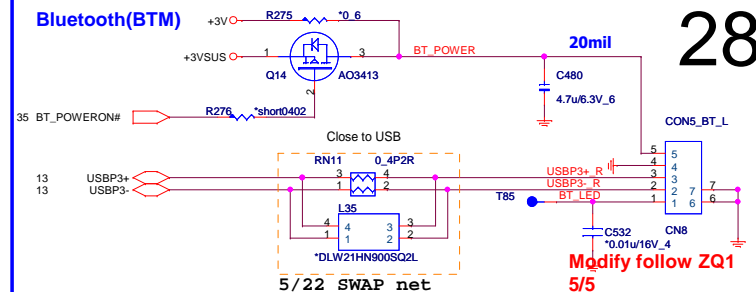
Size	Document Number	Rev
	HDD/ODD/LED/SW/TP/FAN/MMB	1A
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MINI-CARD(MPC)

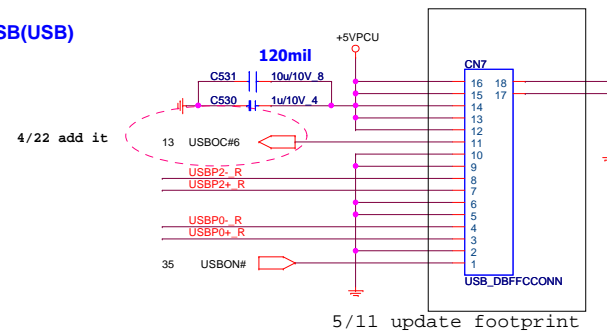
4/21 change footprint andy(ZYD) H=7.0



Bluetooth(BTM)

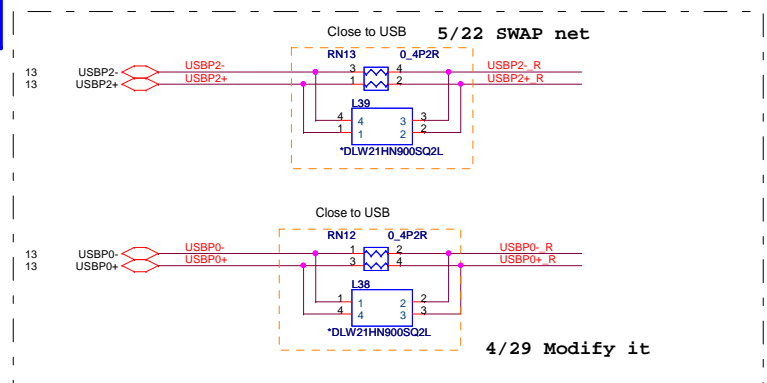
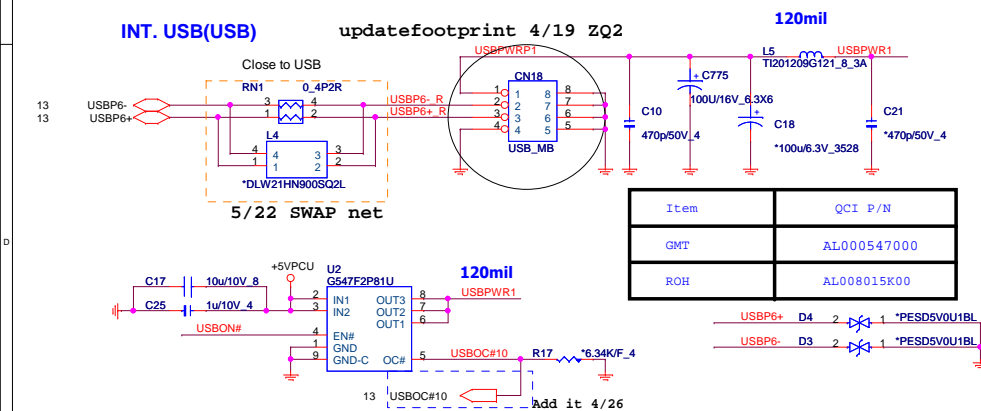


EXT. USB(USB)



INT. USB(USB)

updatefootprint 4/19 ZQ2



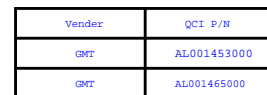
PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number MINI/USB/BT/HOLE	Rev 1A
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HP

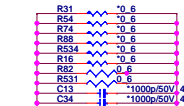


29



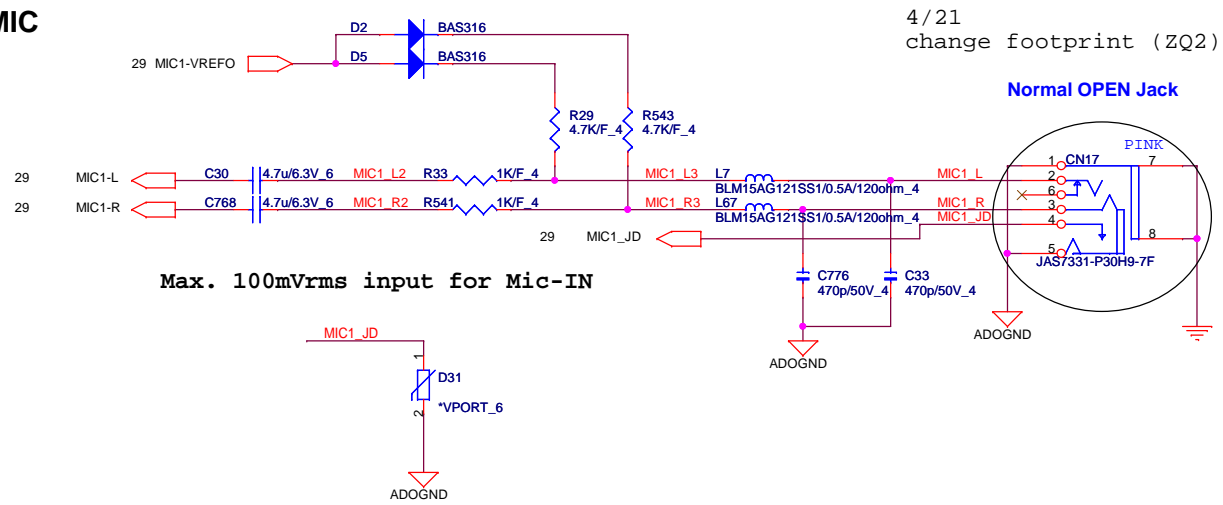
INT MIC

5/26 update Mic Partnumber

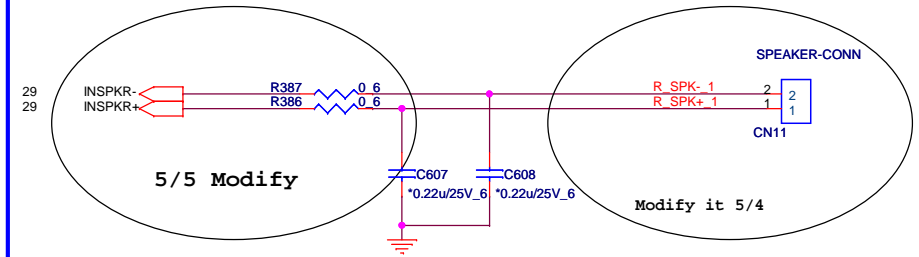


cap place close to MIC-connect

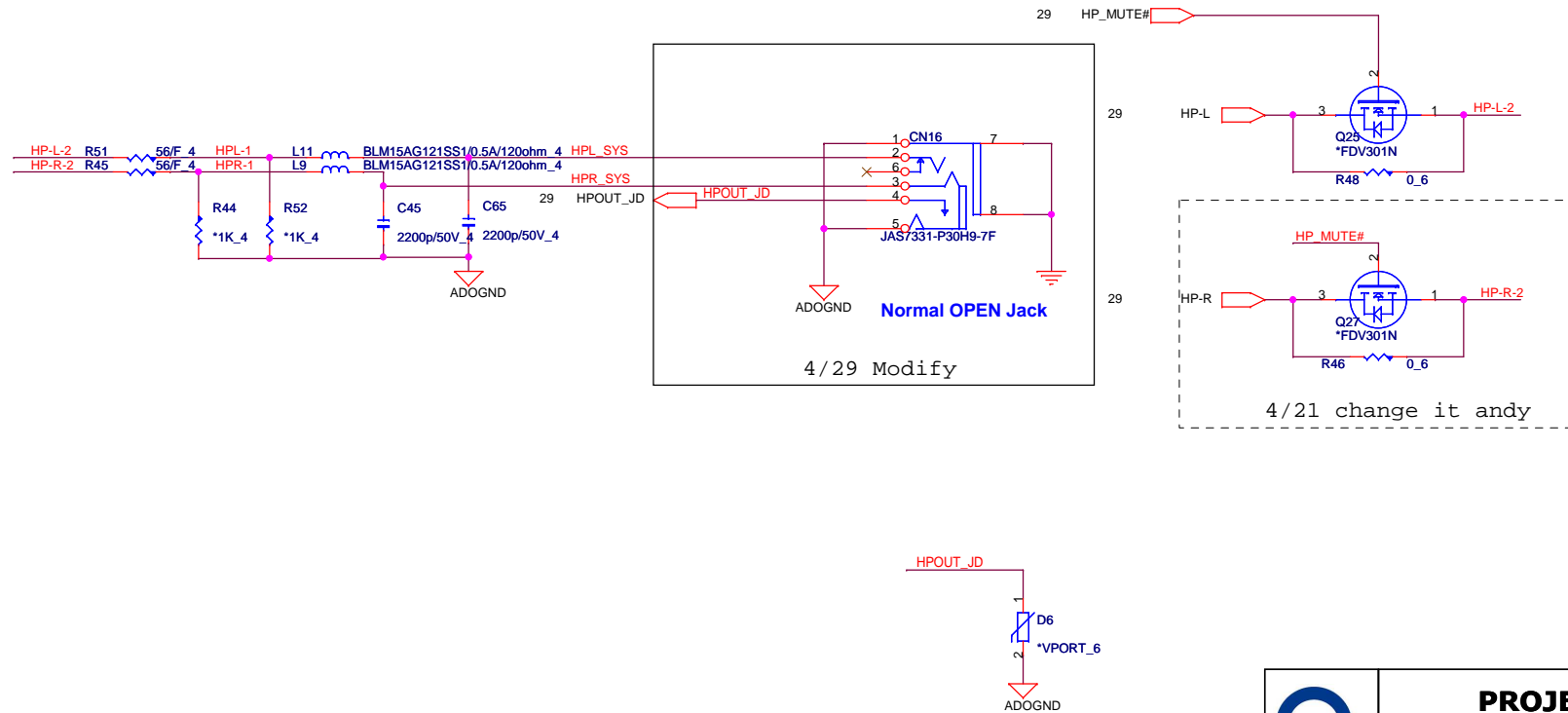
Document Number	Rev
REALTEK ALC663&888/MDC	1A
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Internal Speaker



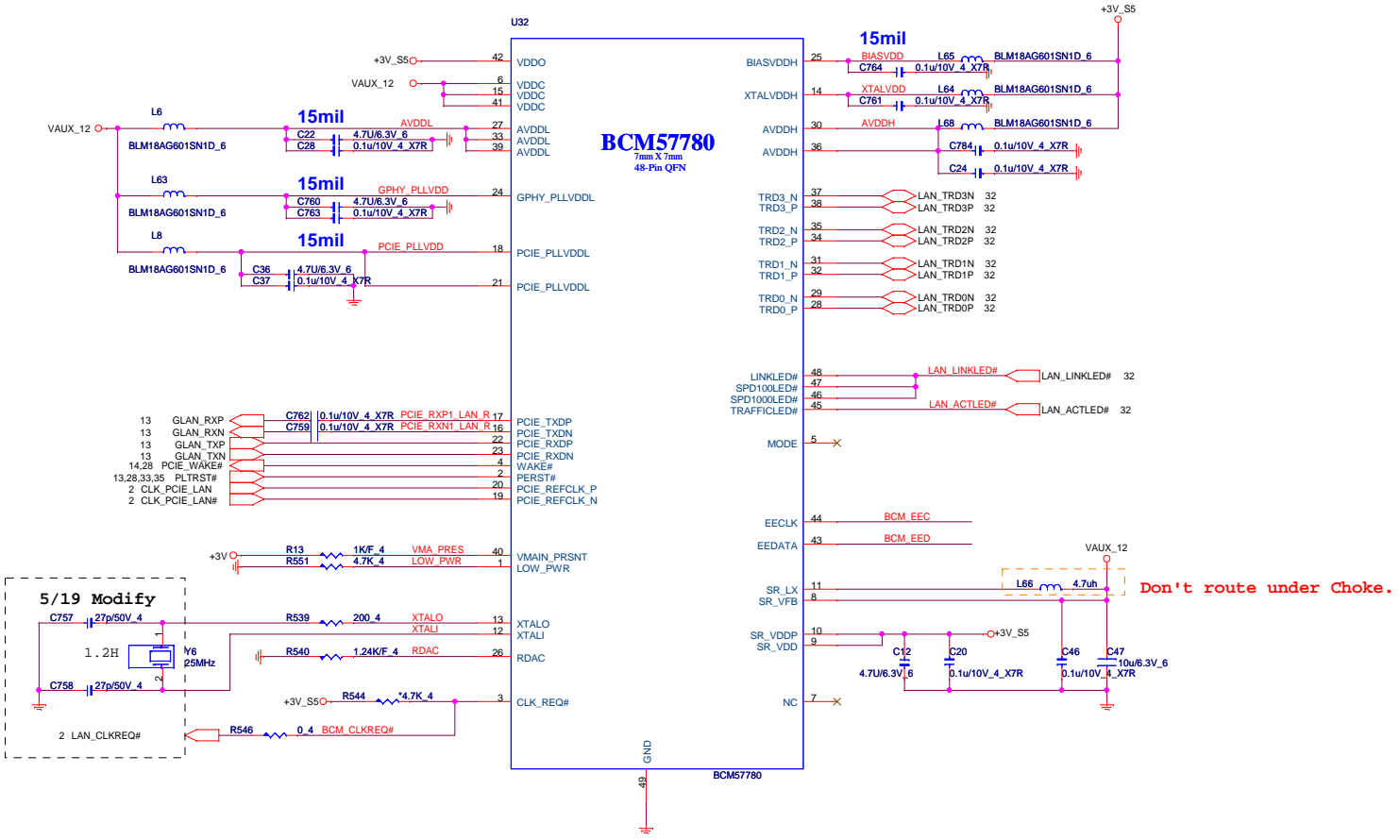
HP/SPDIF



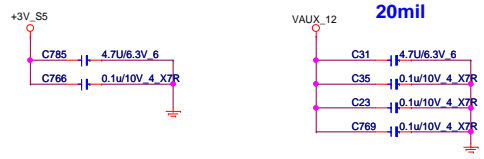
PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	AMP /AUDIO JACK CONN	1A
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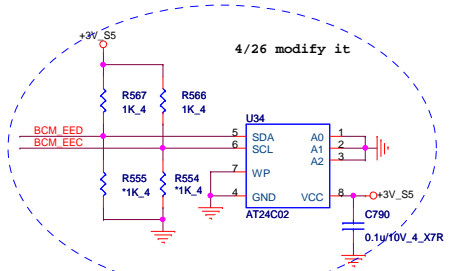
Giga-LAN BCM57780



LAN POWER



EEPROM



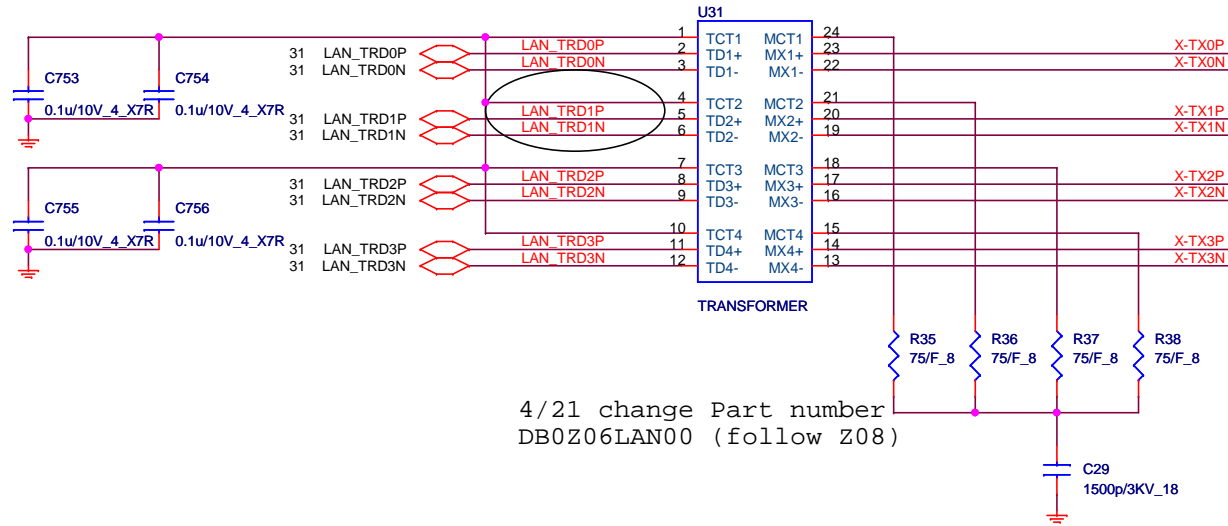
EEPROM Strapping

EEPROM Type	EECLK	EEDATA
24LC02	1	1
Internal	1	0

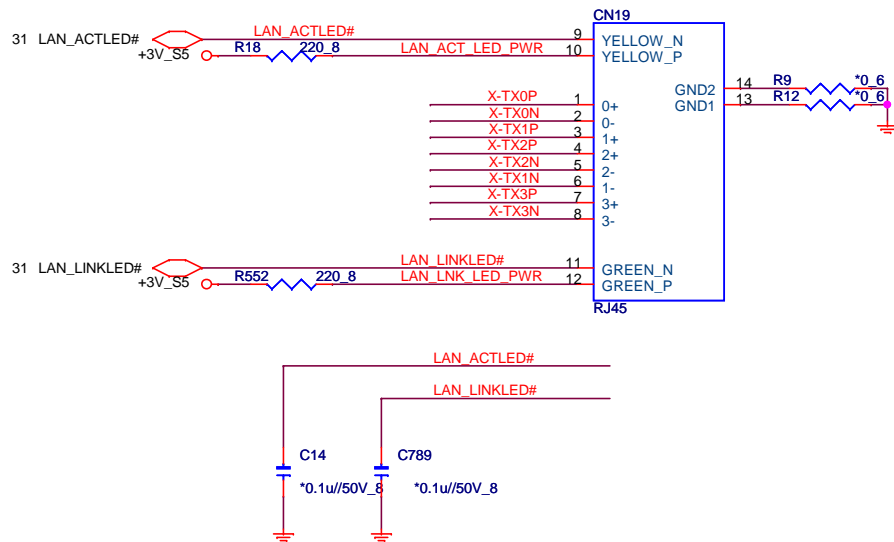
TRANSFORMER

4/27 modify it

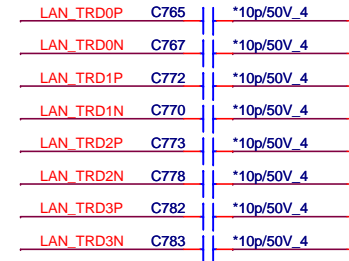
32



RJ45 Conn



For EMI



PROJECT : ZQ5
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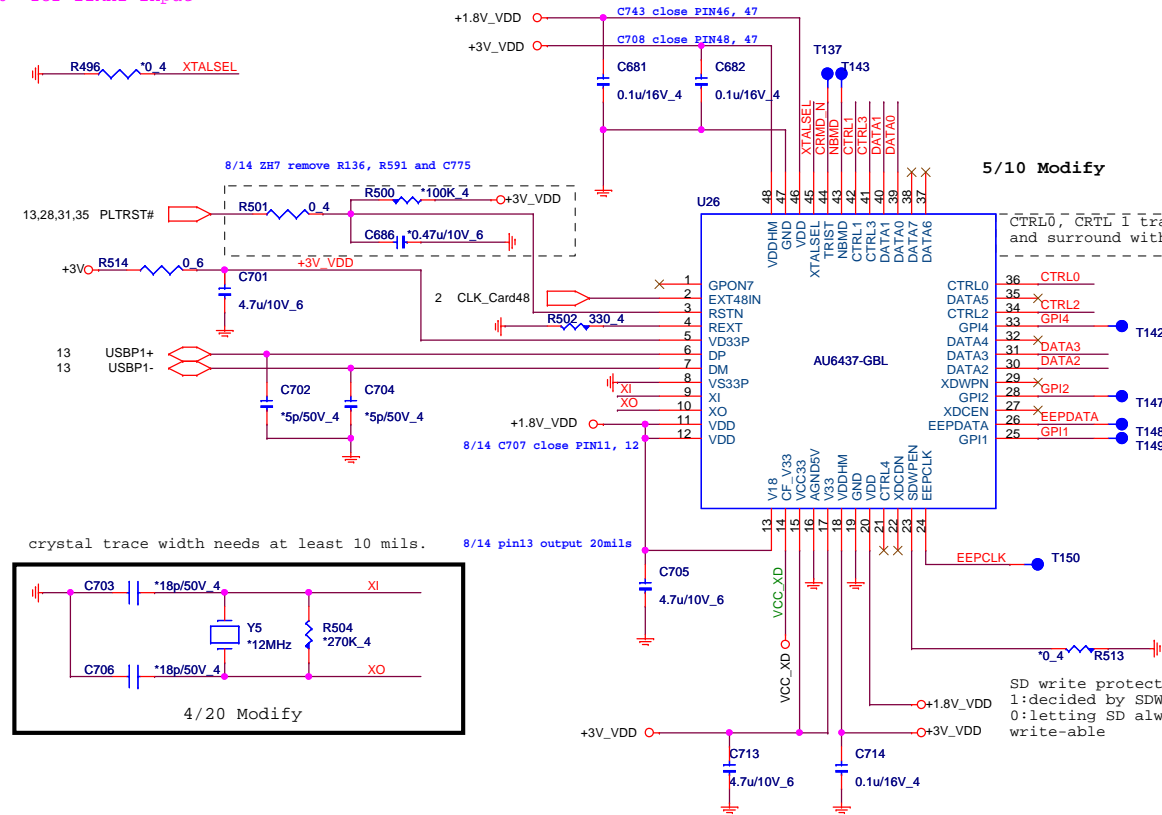
Size	Document Number	Rev
	LAN Transformer and RJ45	1A
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CARD READER Controller

2 IN 1 CARD READER (SD/MMC)

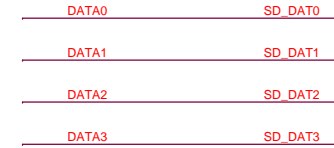
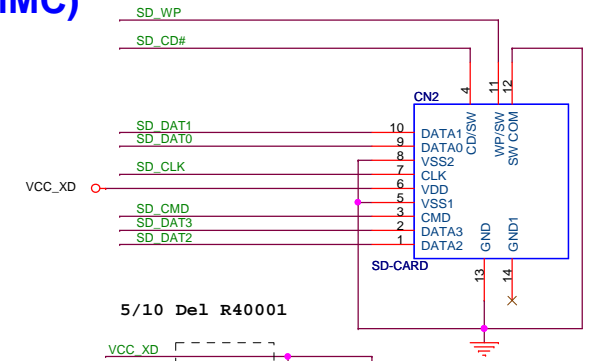
33

Clock input selection
'1' for 48MHz input [Default, Internal PU]
'0' for 12MHz input

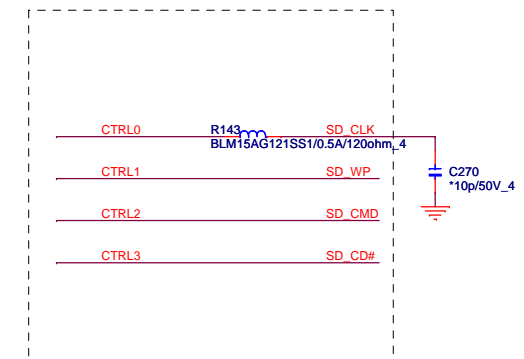


5/10 modify

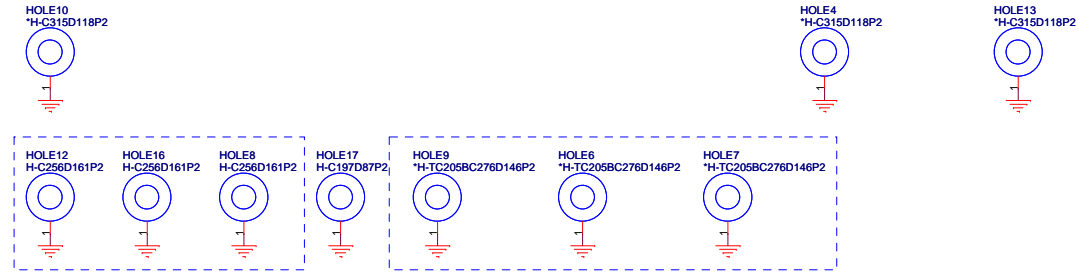
Main	DFHS11FR011
Second	DFHS11FR033



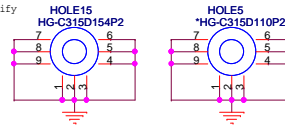
Close to connector



(OTH)

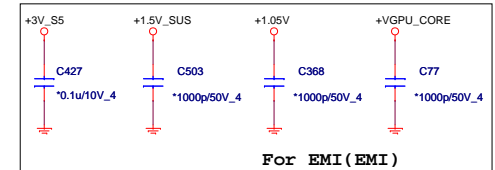
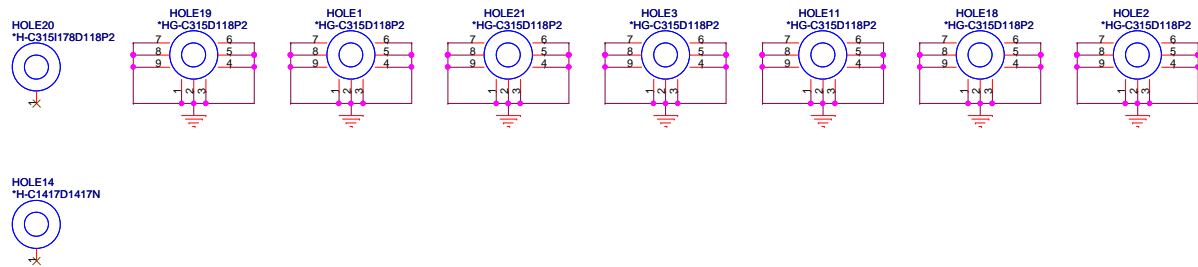


5/21 Modify



5/25 Modify

5/21 Modify



I/O ADDRESS SETTING

SHBM=0: Enable shared memory with host BIOS

SHBM R R289 10K_4

1/13 Confirm by vendor mail :
Disabled ('1') if using FW device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU

Change pull-up resistor (R148 /R144) from 10K to 4.7Kohm

4/20 Modify

2ND MBCLK R285 4.7K_4

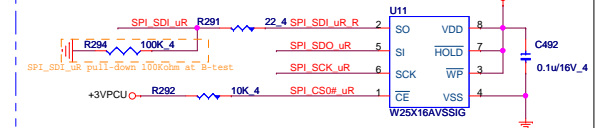
2ND MBDATA R280 4.7K_4

VGA_CLK R297 2.2K_4

VGA_DATA R299 2.2K_4

Modify on 4/19

SPI FLASH

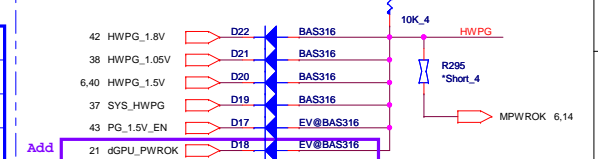


1/13 Confirm by vendor mail :
If the Southbridge enables "Long Wait Abort" by default, the flash device should be 50MHz (or faster)

At 11/24 add Winbond W25X16AVSSIG
MXIC MX25L1605DM2-12G
AMIC A25L016M-F

AKE38FP0N01
AKE38FP0Z00
AKE38ZNB000

HWPG



SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	VGA Thermal
SM Bus 4	

DEL it 5/5

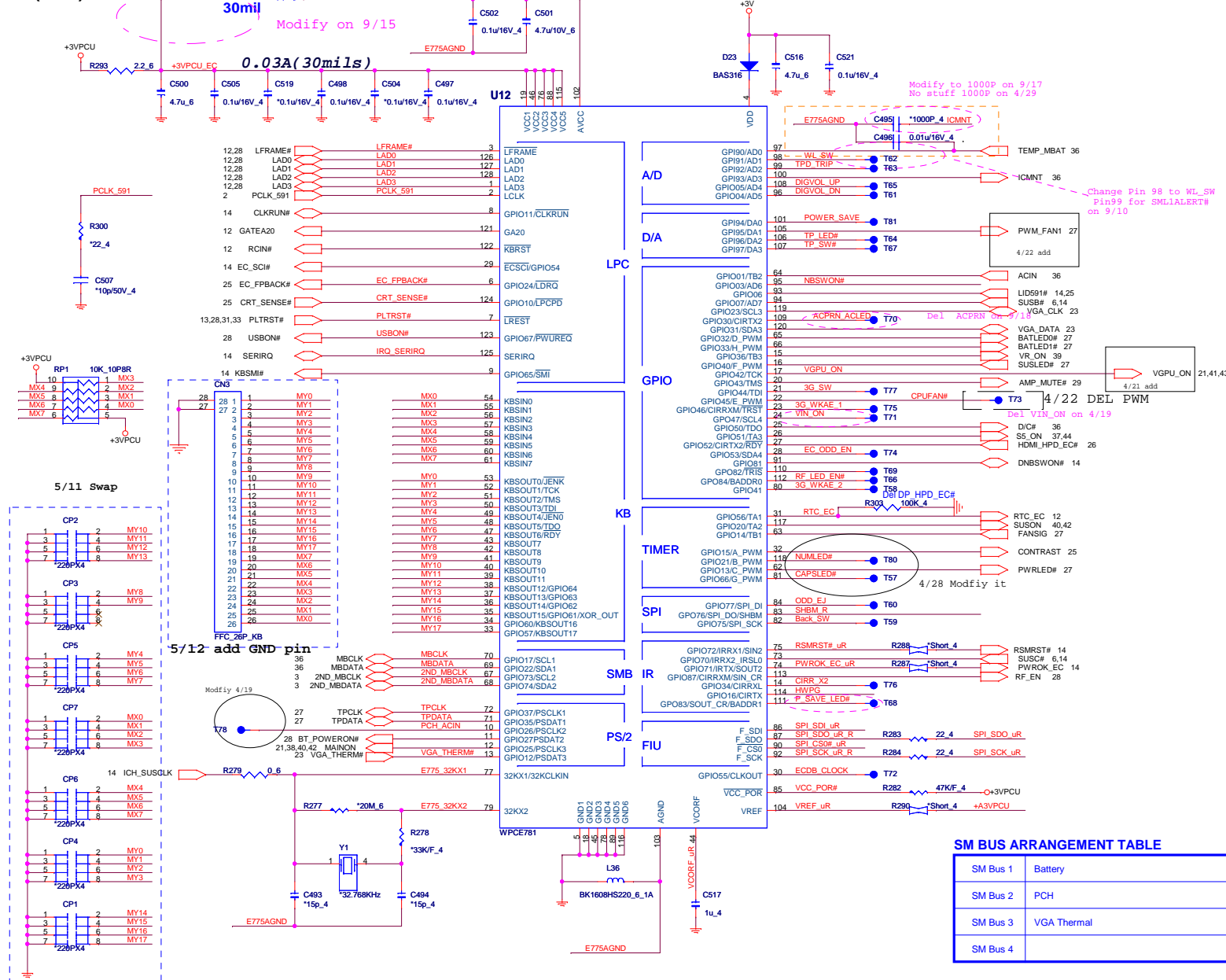
INTERNAL KEYBOARD STRIP SET



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	WPCE81 & FLASH	1A
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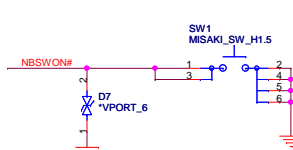
EC(KBC)



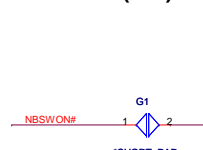
VR Cap.

4/29 DEL VR Cap

POWER-ON Switch



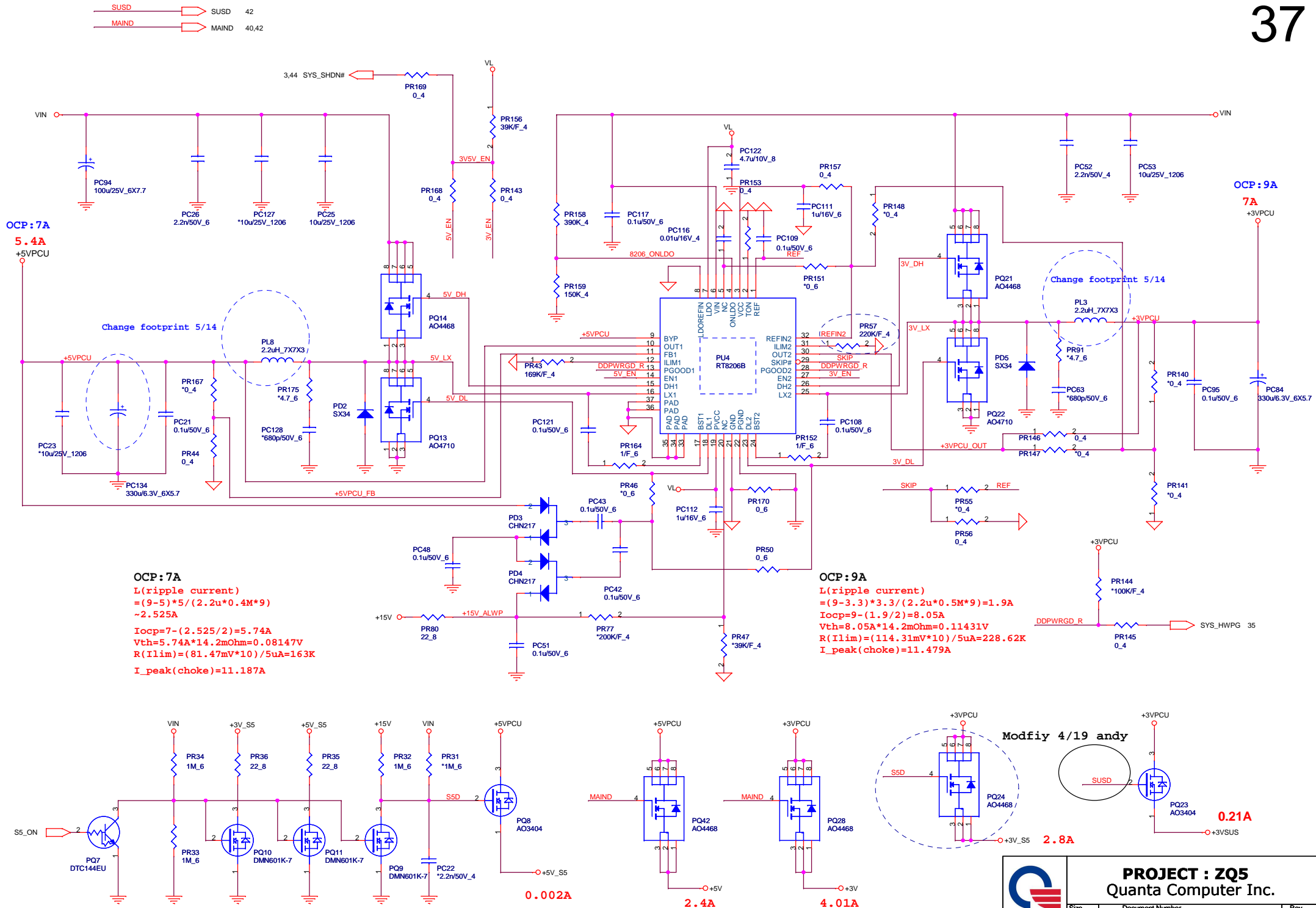
POWER-ON PAD(UIF)



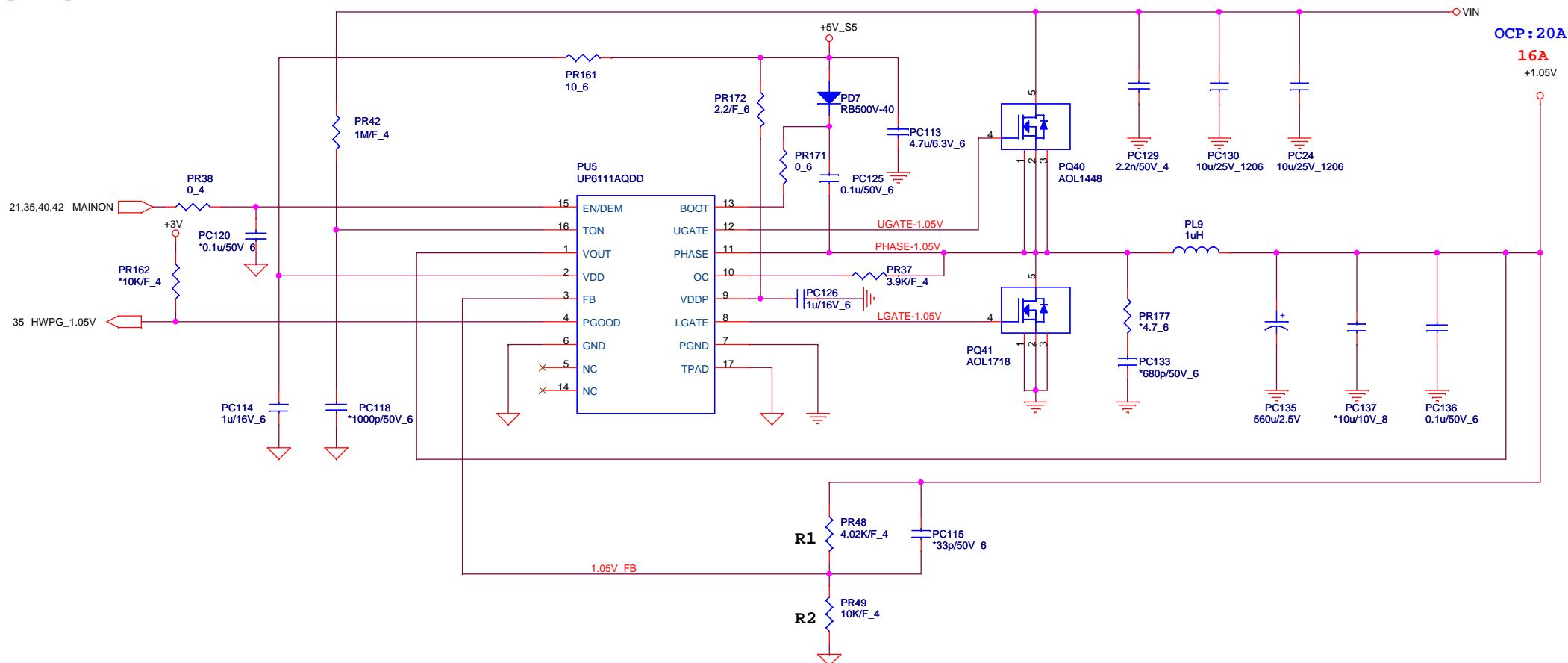
POWER-Smart Key(UIF)

INTERNAL KEYBOARD STRIP SET





[PWM]



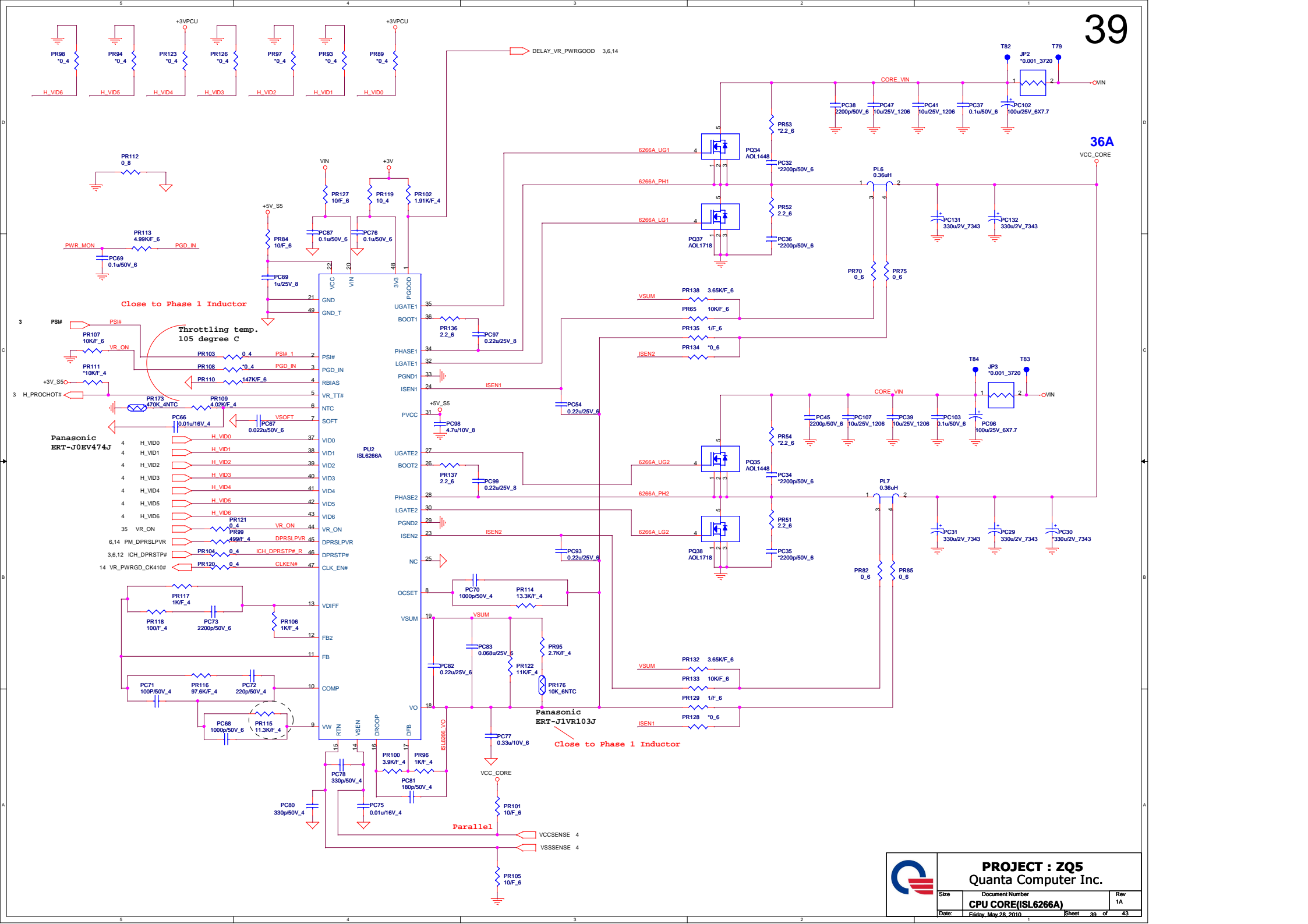
$TON = 3.85p * RTON * Vout / (Vin - 0.5)$
 $Frequency = Vout / (Vin * TON)$
 $TON = 3.85p * 1M * 1 / (Vin - 0.5)$
 $Frequency = 1 / (0.0036767) = 272K$

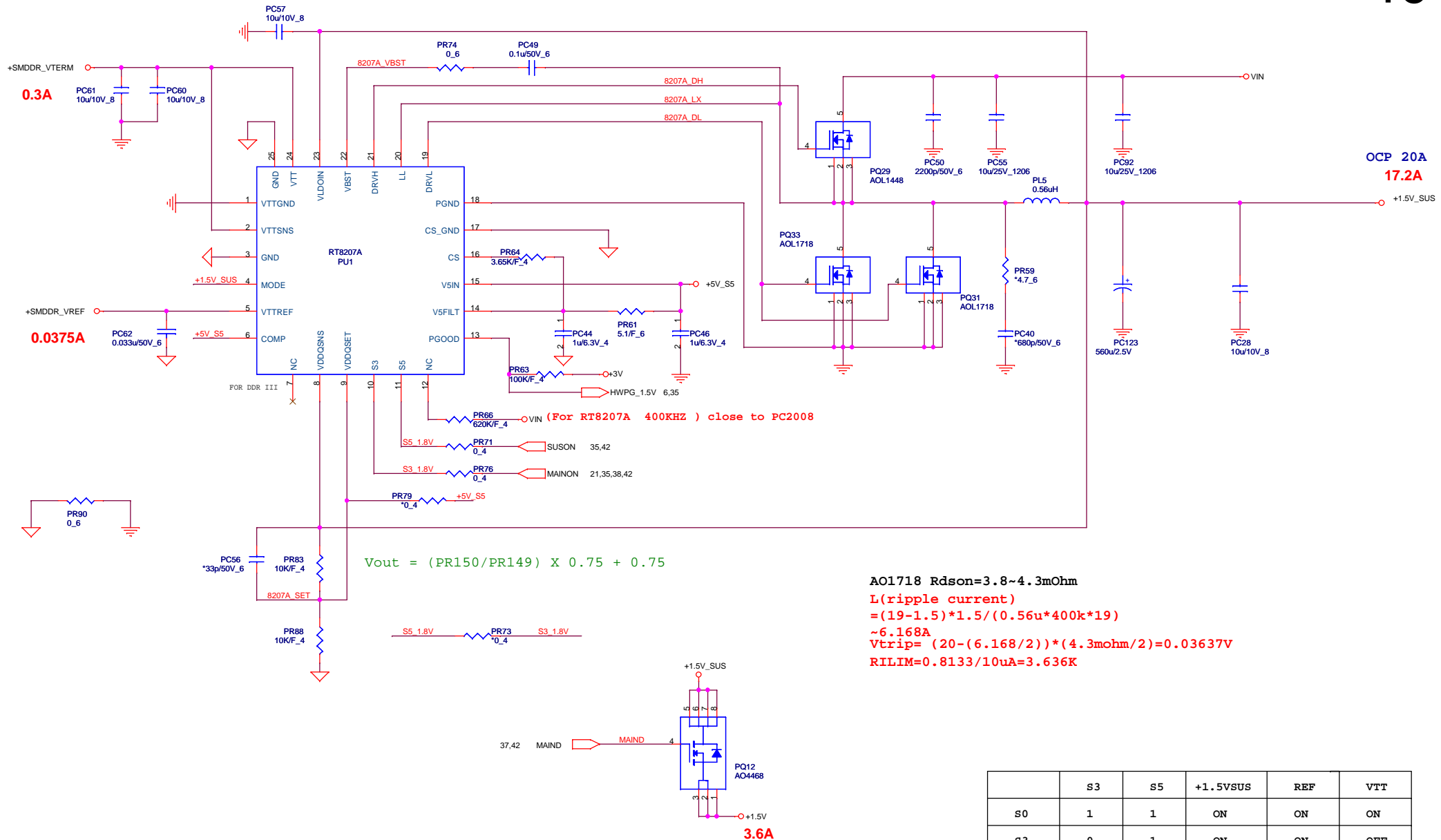
L(ripple current)
 $= (19 - 1.05) \cdot 1.05 / (1 \mu \cdot 272 \text{ k} \cdot 19)$
 $\sim 3.647 \text{ A}$
 $R_{LIM} = 4.3 \text{ m}\Omega \cdot 20 - 1.823 / 20 \mu \text{ A} = 3.907 \text{ K}\Omega$
 $I(\text{choke})_{\text{peak}} = 23.647 \text{ A}$



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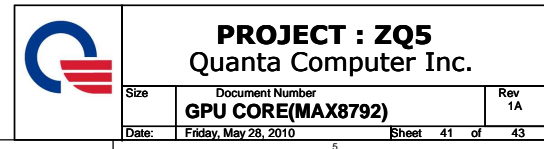


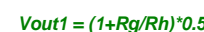
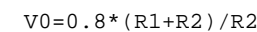
	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF



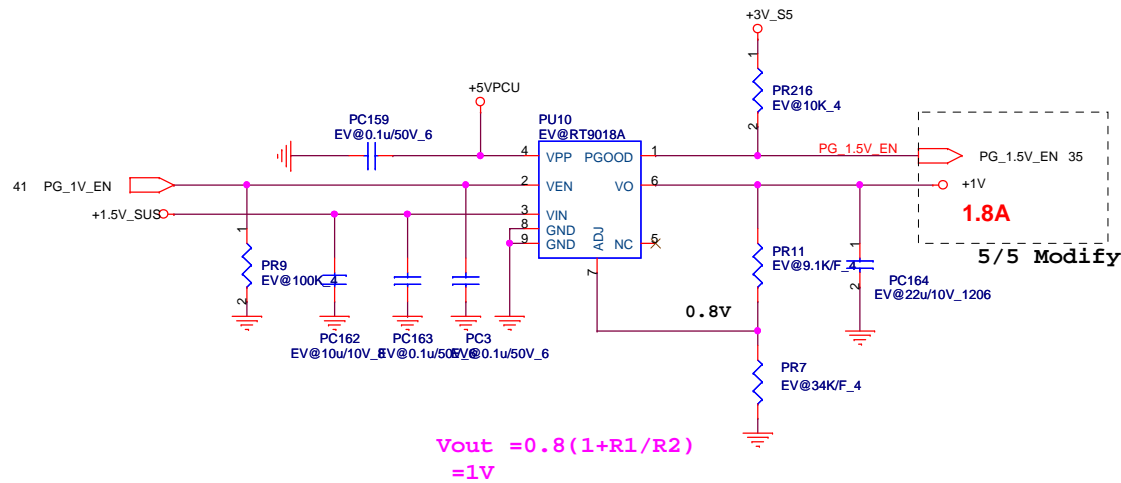
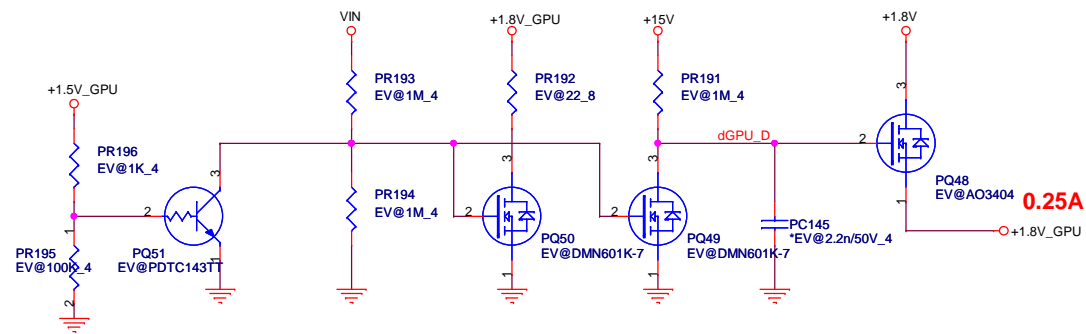
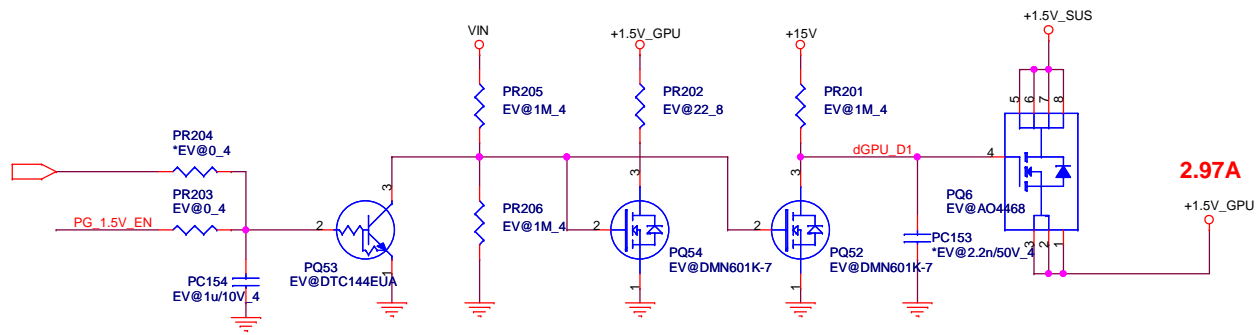
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Quanta Computer Inc.

Size	Document Number	Rev
	DDR 1.5V(TPS51116)	1A
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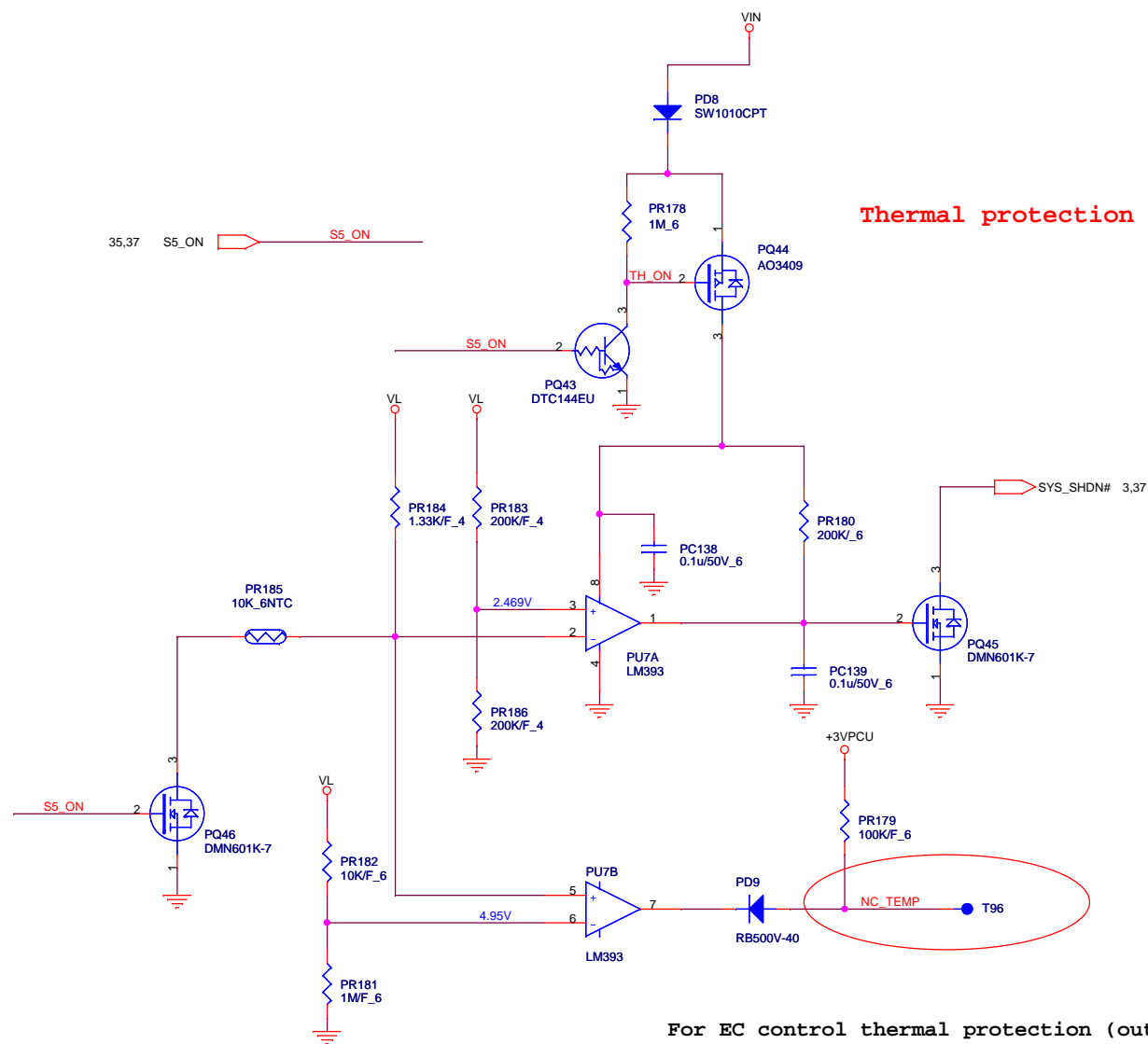


Size	Document Number VCCP 1.8V(UP6111A)	Rev 1A
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	GPU_POWER	1A
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Size	Document Number	Rev 1A
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